

OpenPA **second edition**

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Berlin

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Preface

This is the print edition of the online **OpenPA.net** from Summer 2009.

The OpenPA Project is an independent resource for information on PA-RISC and IA64 computers from HP and other vendors. **This project is independent of and does not represent The Hewlett Packard Company in any way.**

This is the Second Edition 2.3.

Set with L^AT_EX.

Changes in Second Edition 2.3 since Second Edition 2.2:

- ◊ Wax I/O adapter added
- ◊ CPU bus attachments of the PA-RISC processors added
- ◊ Memory and I/O controllers updated and extended
- ◊ HP-UX and other operating system support updated and revised
- ◊ Many pages rewritten and updated with general corrections
- ◊ More price and introduction date information for various HP 9000 systems

All other changes are listed in chapter 5.2.

For the most current version of the OpenPA print edition please refer to <http://www.openpa.net/print.html>.

Thanks

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Chapter 1

Introduction

This book is an informational guide to Hewlett-Packard PA-RISC and IA64 computer systems, architecture and operating systems. PA-RISC is a computer architecture developed by Hewlett-Packard in the early to mid-1980s and used in a long range of HP technical workstations and servers (the various “HP 9000s”). Some systems based on HP/Intel Itanium IA64 are also covered as descendants of the HP 9000/PA-RISC systems.

This book, now in its second edition, is the offspring of the online project OpenPA.net, a non-commercial, central information resource on PA-RISC computers and technical details. It is independent of The Hewlett Packard Company. The online OpenPA.net is a registered serial publication with the ISSN 1866-2757.

Plans for an offline-viewable edition of OpenPA.net for printing-out were first discussed in 2002 but quickly abandoned for lack of technical feasibility and knowledge. A second attempt in 2006 led to the First Edition, published in Summer 2006 and completely updated in November 2007 with Release 1.1 of the First Edition. A limited numbered edition was printed and bound in December of that year, the Release 1.2. Much polishing, content additions (about 90 pages) and updates led to the greatly improved Second Edition in May 2008, quickly followed by 2.1 in October 2008 with more content. Updates included an improved typeset, much polished T_EX usage and much work devoted to tweaking details. More reformatting, several page removals and text overhaul resulted in the Second Edition 2.2 in Winter 2008/2009. The process from the online HTML sources to this PDF is rather long and complicated, with the bulk of the work automated by helper scripts and programs. The only handrolled parts are this introductory chapter, the title/preface pages, the main T_EX file and several manually formatted tables.

The online cousin of this book, OpenPA.net, was founded in 1999 after the author got his first PA-RISC workstation and found almost no coherent information on it and HP PA-RISC on the internet. This bothered him a lot, since other popular Unix/RISC workstation families were thoroughly and well documented (as for example Sun SPARC, DEC MIPS and Alpha). Moreover, at that time many old HP 9000 systems were phased out in favor of new Unix or Windows NT servers resulting in the availability of a lot of used and quite fast PA-RISC computers on the market. The author then spent a lot of time digging through various webpages and the USENET looking for documentation on these systems. After having gathered a considerable amount of information, documentation and references he finally decided to compile this to a webpage and make it publically available, with the first version of the online pages hosted by Bill Bradford of SunHELP. Over the years more PA-RISC computers fell into his hands and he explored other available operating systems, resulting in more details on the site. The support from HP for the PA-RISC Linux project made more interesting documents about PA-RISC internals available. Furthermore, other open-source operating systems for PA-RISC computers made significant progress (primarily OpenBSD/hppa from Michael Shalayeff) so these computers were

used by an increasing amount of people. Documentation on most 64-bit PA-RISC computers (mainly servers, as HP more or less quit producing Unix workstations) and other details were completed in 2007-2008, with only few rare and unusual PA-RISC systems not covered (including the Superdome and other supercomputers). In about the same timeframe a range of IA64/Itanium computers—the PA-RISC successors—were included in OpenPA.net, spanning all three HP Itanium workstations and a big part of HP Itanium servers (the *rx* line).

Chapter 2

PA-RISC Hardware Details

2.1 Overview

An overview on the multiple designs of the PA-RISC platform from the early 1980s to mid-2000s:

1. Early 32-bit systems (1980s TS-1, NS-1, NS-2 and PCX) use custom designs, with most based on SIU/SPI main bus controllers attaching the CPU to the SMB bus. In most cases the system processing and I/O units are made up of a large number of individual chips or boards forming the central chipset. They use CIO and HP-PB expansion buses.
2. PA-7000 and PA-7100 systems use the ASP chipset and Viper memory controller. They utilize the VSC CPU/memory, GSC system main and SGC and EISA expansion buses, with servers using the HP-PB expansion bus, all provided by separate I/O adapters.
3. PA-7100LC and PA-7300LC systems use the highly integrated LASI chipset, which combines most functions and I/O on a single chip, and an on-CPU MIOC memory controller. These systems use GSC or GSC+ as main bus and a variety of expansion buses via bus adapters, ranging from HSC/GSC, EISA to PCI and VME. EISA is provided by Wax, PCI by Dino.
4. PA-7200, PA-8000 and some PA-8200 systems use the U2/Uturn I/O adapters, which attach two GSC/HSC buses to the main Runway bus, and MMC/SMC memory controllers. I/O is realized on the GSC bus with the LASI chipset and Wax and Dino I/O adapters.
5. Some PA-8500, PA-8600 and PA-8700 systems use a “rope”-based architecture with Astro as main system controller and separate Runway+/Runway DDR buses with I/O devices controlled by Elroy PCI bridges.
6. Other 64-bit midrange servers based on the same processors (PA-8500 to 8700) are based on the Stretch chipset, a rather complicated setup with central system controller and links to separate processor and I/O controllers and PCI bridges. Main system bus is the Itanium bus, with converters for the processors’ Runway+/Runway DDR buses.
7. The Superdome “mainframe” and a smaller server, based on PA-8700 and PA-8800/PA-8900 are based on the Cell chipset, similar to the Stretch, but more scalable. Systems are made up of “cells”, with their own central system/memory controller, I/O controller and PCI bridges.
8. The last PA-RISC systems (PA-8800/PA-8900) and several second-generation Itanium systems use the HP zx1 chipset, conceptually similar to Astro systems but with higher data rates and options, based on Itanium 2/McKinley buses.
9. Systems from the Exemplar family as the Convex SPP and HP V-Class are based on the Convex Exemplar crossbar architecture.

2.2 PA-RISC Processors

2.2.1 Introduction

The PA-RISC processors are RISC processors from HP, started in the early 1980s as a replacement for different platforms used in HP computers and developed until the early 2000s. Three major revisions of the PA-RISC architecture were developed:

1. 32-bit MMU-less (no virtual memory) **PA-RISC 1.0**, implemented in several early processors and used in the very first PA-RISC servers;
2. 32-bit **PA-RISC 1.1**, used in the large range of **PA-7x00** processors, and HP 9000 servers and workstations from the late-1980s and 1990s;
3. 64-bit **PA-RISC 2.0**, which extended the 32-bit PA-RISC 1.1 to 64-bit width in the **PA-8x00** processors and featured a redesign of most parts of the architecture, used in the late-1990s and 2000s in the last PA-RISC computers.

Almost all HP Unix systems from the mid-1980 until the early 2000s were based on PA-RISC—other HP product lines (as the HP 3000 systems) and few external integrators (OEMs) used PA-RISC processors as well.

There are roughly five main classes of actual PA-RISC processor designs—two PA-RISC 1.0, two PA-RISC 1.1 and one PA-RISC 2.0, with individual processors mostly being iterations of these basic designs.

- ◇ TS-1, the first PA-RISC processor, PA-RISC 1.0 32-bit, implemented in TTL.
- ◇ NS-1, NS-2 and PCX, the PA-RISC 1.0 32-bit successors. NS-2 tweaked the NS-1 design (both implemented in NMOS) and PCX implemented the NS-2 design on CMOS.
- ◇ PA-7000 and PA-7100, the first PA-RISC 1.1 processors, and the later PA-7100LC and PA-7300LC, integrated “low-cost” PA-RISC 1.1 processors, all 32-bit. The former two have VSC bus system interfaces, with the PA-7000 being the more-integrated descendant of the earlier PCX and the PA-7100 adding superscalarity and integrating the FPU. The two LC processors integrate additional processing logic and direct GSC system bus attachments and on-die memory controllers. The PA-7300LC extended the original PA-7100LC design with true on-chip cache and modified memory controller and bus interfaces.
- ◇ PA-7200, a high-performance PA-RISC 1.1 32-bit processor, a rather large redesign and the first PA-RISC processor with Runway bus interface.
- ◇ PA-8000 and PA-8200, the first PA-RISC 2.0 64-bit processors, were very similar. The subsequent 64-bit processors all were iterations of the basic PA-8000 core. PA-8500, PA-8600 and PA-8700 are direct evolutions of the PA-8000 with large on-chip caches. The PA-8600 and PA-8700 are slight modifications of the PA-8500 with different cache layouts and process technologies. PA-8800 and PA-8900 implemented dual PA-8700 cores onto single-dies with large off-die but on-chip caches.

Several third-party vendors designed and produced PA-RISC processors under license, including the general-purpose CPUs from Hitachi (PA/50 and HARP) and various microcontrollers from Winbond and Oki.

2.2.2 Overview table

Table 2.1: PA-RISC processors overview

CPU	ISA	Clock max	FETs	L1 Cache max	L2 Cache max	Bus	Super scalar	SMP	Units
TS-1	PA 1.0 32-bit	8MHz	?	128KB I/D <i>off-chip</i>		Custom	1-way	No	1 Integer External FPU
NS-1	PA 1.0 32-bit	30MHz	144k	128KB <i>off-chip</i>		SMB	1-way	No	1 Integer External FPU
NS-2	PA 1.0 32-bit	27.5MHz	183k	1MB I/D <i>off-chip</i>		SMB	1-way	Yes	1 Integer External FPU
PCX	PA 1.0 32-bit	50MHz	196k	1MB I/D <i>off-chip</i>		SMB	1-way	Yes	1 Integer External FPU
PA-7000	PA 1.1a 32-bit	66MHz	577k	256KB I 256KB D <i>off-chip</i>		PBus/VSC	1-way	No	1 Integer External FPU
PA-7100/ PA-7150	PA 1.1b 32-bit	125MHz	850k	1MB I 2MB D <i>off-chip</i>		PBus/VSC	2-way	Yes	1 Integer 1 Floating Point
PA-7100LC	PA 1.1c 32-bit	100MHz	900k	1KB I <i>on-chip</i>	2MB <i>off-chip</i>	GSC	2-way	No	2 Integer 1 Floating Point MAX-1
PA-7200	PA 1.1d 32-bit	140MHz	1.3M	2KB <i>on-chip</i>	1MB I 2MB D <i>off-chip</i>	Runway	2-way	Yes	2 Integer 1 Floating Point
PA-7300LC	PA 1.1e 32-bit	180MHz	9.2M	64KB I 64KB D <i>on-chip</i>	8MB <i>off-chip</i>	GSC	2-way	No	2 Integer 1 Floating Point MAX-1
PA-8000	PA 2.0 64-bit	230MHz	4.5M	1MB I 1MB D <i>off-chip</i>		Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8200	PA 2.0 64-bit	300MHz	4.5M	2MB I 2MB D <i>off-chip</i>		Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8500	PA 2.0 64-bit	440MHz	140M	512KB I 1MB D <i>on-chip</i>		Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8600	PA 2.0 64-bit	550MHz	140M	512KB I 1MB D <i>on-chip</i>		Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8700	PA 2.0 64-bit	875MHz	186M	768KB I 1.5MB D <i>on-chip</i>		Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8800 2-core	PA 2.0 64-bit	1GHz	300M	2× 768KB I 768KB D <i>on-chip</i>	32MB <i>off-chip</i>	Itanium 2	2× 4-way	Yes	2× 4 Integer 4 Floating Point 2 Load/Store MAX-2
PA-8900 2-core	PA 2.0 64-bit	1.1GHz	317M	2× 768KB I 768KB D <i>on-chip</i>	64MB <i>off-chip</i>	Itanium 2	2× 4-way	Yes	2× 4 Integer 4 Floating Point 2 Load/Store MAX-2

Hitachi PA/50	PA 1.1 32-bit	60MHz	1.28M	8KB I 4KB D <i>on-chip</i>		?	1-way?	No?	1 Integer 1 Floating Point
Hitachi HARP-1	PA 1.1 32-bit	150MHz	2.8M	8KB I 16KB D <i>on-chip</i>	512KB I 512KB D <i>off-chip</i>	?	2-way	No?	2 Integer 1 Floating Point (<i>Vector</i>)

Table Notes

- ◇ **ISA:** Instruction set architecture—version of the PA-RISC architecture and its *width*, i.e. integer register width and maximum addressable memory (32-bit or 64-bit)
- ◇ **FETs:** Number of transistors
- ◇ **L1/L2 Caches:** Maximum amount of Level 1 and Level 2 cache memories—*on-chip* is integrated onto the CPU die while *off-chip* cache is implemented with separate chips (most PA-RISC processors supported larger off-chip caches than were implemented in actual products)
- ◇ **Bus:** Type of bus the processor attaches to on the main board (note that this is in two cases the main I/O bus [GSC on the LC processors] and on the others the processor/memory bus)
- ◇ **SMP:** Capability of the CPU to work in multi-processor configuration
- ◇ **Units:** Number of functional processing units, for integer and floating point arithmetic, and load/store operations. Also notes if the MAX multimedia extensions are available.

2.2.3 Early PA-RISC

The first PA-RISC processors, designed and used in the mid to late-1980s in the HP 9000/800 servers (and HP 3000 MPE/iX systems), are very poorly documented. Their exact nomenclature is not clear, one group of sources refers to them as TS-1, NS-1 and NS-2, while other call apparently the same processors PN-5, PN-7 and PN-10. These early CPUs still mostly were *chipsets*—multiple separate chips and components formed the central processing unit, contrary to the mostly single-chip post-PA-7000 implementations. The chips were based first on TTL, then NMOS-III and finally CMOS26B. An interesting aspect of these CPUs are their huge TLB sizes—from 2048 up to 16384 entries while their successors and competitors had sizes typically in the low to mid hundreds.

TS-1

Used in: 840

Introduced in: 1986

The TS-1 was the very first PA-RISC production processor and integrated version 1.0 of PA-RISC on six boards (each 8.4×11.3") of TTL.

Details:

- ◇ PA-RISC version 1.0 32-bit
- ◇ Three-stage pipeline
- ◇ The CPU consists of six separate boards:
 1. I-unit: the Instruction Unit
 2. Register File Board, contains general and control registers
 3. E-unit: the Execution Unit

- 4. TLB, the translation lookaside buffer with 4096 entries for 2KB pages
- 5. Cache controller with split instruction and data caches—64KB for each I and D
- 6. FPC, the floating-point coprocessor, handles FP operations parallel to the CPU/ALU (the ADD/MUL/DIV chip was taken over from the HP 9000/550 FOCUS system)
- ◇ 4096-entry TLB off-chip, direct-mapped
- ◇ Off-chip L1 cache of 128KB (I/D) direct-mapped/one-way associative
- ◇ Physical address space of 27-bit (128MB main memory could be addressed)
- ◇ 8MHz clock speed
- ◇ Six (some sources say five) printed circuit boards, implemented in FAST TTL and (25ns and 35ns) SRAMs/PALs, which each about 150 ICs

NS-1

Used in: 825, 835, 850

Introduced in: 1987

The first implementation of PA-RISC in a NMOS fabrication process followed shortly on the original TTL-based TS-1 and was called NS-1. The NS-1 processor is integrated on one circuit board (two on 825 server) with the CPU as single NMOS-III chip supplemented by external support chips:

Details:

- ◇ PA-RISC version 1.0 32-bit
- ◇ Three-stage pipeline
- ◇ CPU is a single chip, with eight support VLSI chips
 1. SIU (system interface unit), attaches the CPU to the SMB main bus
 2. two CCUs (cache controller units CCU0 and CCU1), attach to separate external cache chips
 3. TCU (TLB controller unit), attaches to the external TLB chips
 4. MIU (math interface unit), controls three third-party floating point (FP) chips (ADD, MUL and DIV)
- ◇ 2048 to 4096-entry TLB off-chip
- ◇ Off-chip L1 cache of 16KB (HP 9000/825) to 128KB (others), unified
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ CPU attaches via System Main Bus (SMB) to memory and I/O (controllers)
SMB is a synchronous, pipelined bus with 64-bit wide address and data transfers
- ◇ 25-30MHz clock speed
- ◇ One circuit board (two boards on HP 9000/825), 144,000 FETs, implemented in NMOS-III packaged in a 272-pin ceramic PGA package

NS-2

Used in: 822, 832, 845, 855, 860

Introduced in: 1989-1990

The final NMOS PA-RISC processor was the NS-2, a tweaked follow-on to the NS-1 with increased pipeline stages (from three to five), new TLB and cache controllers and significantly larger caches and TLB. The NS-2 design was simplified over its NS-1 predecessor. The processor is implemented on one circuit board with the CPU as a single NMOS-III and seven other VLSI chips. The bus structure connecting these chips was updated and simplified, with the CPU having private connections to the cache and TLB controllers (for which the NS-1 CPU had to use the shared cache bus).

Details:

- ◇ PA-RISC version 1.0 32-bit
- ◇ CPU is a single chip with seven VLSI support chips
 1. SIU (system interface unit), attaches the CPU to the SMB main bus
 2. two CCUs (cache controller units, split into instruction and data—ICCU and DCCU), attach to separate external cache chips
 3. TCU (TLB controller unit), attaches to the external TLB chips
 4. FPC (floating point controller), controls two third-party floating point (FP) chips (ADD, MULTI)
- ◇ Five-stage pipeline
- ◇ 16384-entry TLB off-chip
- ◇ Off-chip L1 cache up to 1024KB, split into I/D
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ CPU attaches via System Main Bus (SMB) to memory and I/O (controllers)
SMB is a synchronous, pipelined bus with 64-bit wide address and data transfers
- ◇ 27.5MHz clock speed (or maximum of 30MHz?), power dissipation of 26W
- ◇ One circuit board, CPU implemented in NMOS-III, 183,000 FETs, 1.5µNMOS-III, die size 14.0×14.0 mm² die, packaged in 408-pin PGA

PCX (CMOS26B)

Used in: 842, 852, 865, 870

Introduced in: 1990?

The last PA-RISC 1.0 design was the CMOS26B or PCX and the first PA-RISC processor fabricated in a CMOS process. It implemented the NS-1/NS-2 NMOS design and several of the processor functions previously supplied on external VLSI chips onto a single CPU chip. The PCX still was supplemented by external support chips, including three CMUX (cache multiplexer—one instruction, two data; equivalent to the earlier CCUs), SPI (SMB to processor interface—SMB is the system main bus), FPC (floating point coprocessor) and two FP chips (MUL/DIV and ADD/SUB) [*not completely clear if the latter two or latter three chips are third-party*].

- ◇ PA-RISC version 1.0 32-bit

- ◇ First multi-processor-capable PA-RISC CPU (up to four-way SMP)
- ◇ Direct predecessor of the PA-7000 (PCXS) processor which integrated most processor logic minus the FPU onto a single die/chip
- ◇ External FPU (apparently ECL logic)
- ◇ 8192-entry TLB on-chip
- ◇ Off-chip L1 cache up to 1024KB, split into I/D (apparently asymmetrical 1:2 I/D)
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ CPU attaches via System Main Bus (SMB) to memory and I/O (controllers)
SMB is a synchronous, pipelined bus with 64-bit wide address and data transfers
- ◇ 50MHz clock speed
- ◇ One circuit board, 196,000 FETs, 1.0μ(micron), implemented in three-level CMOS (CMOS26B)
- ◇ CPU is a single chip, needs seven other (VLSI) support chips for memory/bus interfaces and I/O

There are sources which also mention a “CS-1” processor — from the nomenclature this would point to a CMOS design but the performance figures/charts do not really match up with the CMOS26B/PCX described here.

References

1. Wayne E. Holt (ed.), *Beyond RISC! An Essential Guide to Hewlett-Packard Precision Architecture* (January 1988: Software Research Northwest Inc.)
2. **Hardware Design of the First HP Precision Architecture Computers¹** (PDF) David A. Fotland et al (March 1987: Hewlett-Packard Journal)
3. **HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook²** (PDF) Hewlett-Packard Company (October 1990. Accessed January 2008 at hpmuseum.net)
4. **HP 9000 Series 800 Model 825S Hardware Technical Data³** (PDF) Hewlett-Packard Company (September 1988. Accessed January 2008 at hpmuseum.net)
5. **HP 3000/925 and HP 9000/825/835 Computer Systems CE Handbook⁴** (PDF) Hewlett-Packard Company (May 1988. Accessed January 2008 at hpmuseum.net)
6. **New midrange members of the Hewlett-Packard Precision Architecture Computer Family⁵** Thomas O. Meyer et al (June 1989: Hewlett Packard Journal. Accessed January 2008 at findarticles.com)
7. **HP 9000 Series 800 Model 822S/832S Technical Data⁶** (PDF) Hewlett-Packard Company (1989. Accessed January 2008 at hpmuseum.net)
8. *A 30 MIPS VLSI CPU*, Brian D. Boschma et al (ISSCC 89: February 1989)

¹ <http://hpmuseum.net/document.php?catfile=372>

² <http://www.hpmuseum.net/document.php?hwfile=4049>

³ <http://www.hpmuseum.net/document.php?hwfile=3343>

⁴ <http://www.hpmuseum.net/document.php?hwfile=4048>

⁵ http://findarticles.com/p/articles/mi_moHPJ/is_n3_v40/ai_7397316

⁶ <http://www.hpmuseum.net/document.php?hwfile=2652>

2.2.4 PA-7000 (PCX-S) (*Cheetah*)

Used in

- ◇ 705, 710, 720, 730, 750
- ◇ F10, F20, F30, G30, G40, H20, H30, H40, I30, I40
- ◇ Mitsubishi ME/R7200, ME/S7200, ME/R7300, ME/S7300, ME/R7500, ME/S7500

Time of introduction

1991

Overview

The PA-7000 was the first PA-RISC version 1.1 processor and first used in the new *700 series workstations* and later in some of the *Nova* servers. The PA-7000 is a multi-chip implementation:

- ◇ Central CPU with ALU, TLB and the I/D cache controllers
- ◇ Viper Memory and I/O Controller (MIOC)
- ◇ External FPU
- ◇ PBus/VSC interface, buffer chips for data/addresses between VSC and PBus

Details

- ◇ PA-RISC version 1.1a 32-bit
- ◇ Needs external FPU (commonly used was a coprocessor developed by HP and Texas Instruments)
- ◇ Five-stage pipeline
- ◇ 96/96 I/D TLB
- ◇ 4/4 I/D BTLB
- ◇ 32-bit bus to I cache
64-bit bus to D cache
- ◇ PBus 32-bit from processor to the Memory and I/O Controller (MIOC)
- ◇ Off-chip caches up to 256KB/256KB I/D
- ◇ Up to 66MHz frequency with 5.0V core voltage
- ◇ 14.2×14.2 mm² die, 577,000 FETs, 1.0μ(micron), 2-layer CMOS (CMOS26B) in 408-pin CPGA
- ◇ External FPU fabbed in 13.0×13.0 mm² die, 640,000 FETs, 0.8μ(micron), TI EPIC-2 in 207-pin CPGA

References

1. Various
2. Évolution des gammes de processeurs MIPS, DEC Alpha, PowerPC, SPARC, x86 et PA-RISC⁷ (PDF) André Seznec and Thierry Lafage (INRIA: June 1997)
3. Midrange PA-RISC Workstations with Price/Performance Leadership⁸ (.pdf) pp. 6-11 Andrew J. DeBaets and Kathleen M. Wheeler (August 1992: Hewlett-Packard Journal)
4. VLSI Circuits for Low-End and Midrange PA-RISC Computers⁹ (.pdf) pp. 12-22 Craig A. Gleason (August 1992: Hewlett-Packard Journal)

2.2.5 PA-7100/PA-7150 (PCX-T) (*Thunderbird*)

Used in

- ◇ 715, 725, 735, 755
- ◇ 742i, 745i, 747i
- ◇ G50, G60, G70, H50, H60, H70, I50, I60, I70
- ◇ T500, T520
- ◇ Convex SPP1000/CD, SPP1000/XA
- ◇ Hitachi 3050RX 220, 230, 310S, 320, 330, 430, 440, 9000V V735/I25, VT500
- ◇ Stratus Continuum 610S, 610, 615S, 615, 620, 625, 1220, 1225, 1245

Time of introduction

Early 1992 (PA-7150: 1994)

Overview

The PA-7100 the first PA-RISC CPU to integrate the ALU and FPU on a single die, saving board space and lowering production cost. The design of the basic and integer units is close to the PA-7000, which was modified to scale to higher frequencies; the (previously external) FPU was a new design, taking about one third of the transistor count. The link between the PA-7100 and its instruction cache has been doubled compared to the PA-7000, which enables the CPU to fetch multiple consecutive instructions and simultaneously dispatche them to independent integer and floating point units. The PA-7100 is a superscalar processor that is able to issue two separate instructions at a time.

SMP systems can be built with two alternative strategies: either two PA-7100s attach via a shared PBus to one Memory and I/O Controller (Viper) to which the system bus and memory separately attach; or each PA-7100 is attached to its own MIOC, which in turn is attached to a shared memory and I/O bus with the other PA-7100/MIOCs.

⁷ <ftp://ftp.inria.fr/INRIA/publication/publi-pdf/RR/RR-3188.pdf>

⁸ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

⁹ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

The PA-7150 is a PA-7100 with tweaks to the core and cache subsystem to allow clock frequencies up to 125MHz.

The PA-7100 was hardware developed on an HP 9000/I-Class server.

Details

- ◇ PA-RISC version 1.1b 32-bit
- ◇ Two functional units: 1 integer ALU, 1 Floating Point unit
- ◇ 2-way superscalar
- ◇ SMP-capable
- ◇ CPU, FPU, MMU and cache controller on one chip, memory and I/O controller (Viper MIOC) off-chip
- ◇ Five-stage pipeline
- ◇ *Pipeline store* technique for reduction of penalty for execution of any store to data cache
- ◇ *Stall-on-use* mechanism for parallel procession of instruction streams and cache misses
- ◇ 3-instruction queue
- ◇ Hardware TLB miss handler
- ◇ Hardware static branch support
- ◇ I/D cache bypass (7150)
- ◇ Off-chip L1 caches up to 1MB I and 2MB D realized in asynchronous standard SRAMs
- ◇ I/D caches are both 64-bit per access, direct mapped, parity protected and cycled at CPU clock
- ◇ Caches are attached directly to the CPU
- ◇ Caches are software accessible
- ◇ Caches are virtually indexed and physically tagged to minimize latency
- ◇ 120-entry fully associative TLB
- ◇ 16-entry BTLB with programmable page sizes up to 64MB
- ◇ CPU attaches via PBus to the Viper memory and I/O controller (MIOC)
- ◇ PBus is 32-bit multiplexed address/data bus and probably runs at possible bus speeds of 1.0, .67 and .50 of processor speed
- ◇ Two different multiprocessing connection strategies supported (shared MIOC or dedicated MIOCs)
- ◇ MP cache coherency support
- ◇ Up to 100MHz frequency (PA-7100) with 5.0V core voltage
- ◇ Up to 125MHz frequency (PA-7150) with 5.0V core voltage
- ◇ 14.0×14.0 mm² die, 850,000 FETs, 0.8μ(micron), 3-layer metal CMOS (CMOS26B process) packaged in a 504-pin ceramic PGA package
- ◇ Power dissipation of 30W at 100MHz

References

1. Various
2. **A 200 MFLOP HP PA-RISC Processor**¹⁰ (.pdf) W. Jaffe, B. Miller, J. Yetter (1992: Hewlett Packard. Proceedings of IEEE Hot Chips IV)
3. **Multiprocessor Features in a PA-RISC Processor Interface Chip**¹¹ (.pdf) T. Alexander et al (1992: Hewlett Packard. Proceedings of IEEE Hot Chips IV)
4. **Évolution des gammes de processeurs MIPS, DEC Alpha, PowerPC, SPARC, x86 et PA-RISC**¹² (PDF) André Seznec and Thierry Lafage (INRIA: June 1997)

2.2.6 PA-7100LC (PCX-L) (*Hummingbird*)

Used in

- ◇ 712, 715, 725
- ◇ 743i, 748i
- ◇ D200, D210, D300, D310
- ◇ E25, E35, E45, E55
- ◇ Hitachi 3050RX 225, 235, 255, 535, e9000V V715, V715Tiny, VE25, VE35, VE45, VE55
- ◇ SAIC Galaxy 1100

Time of introduction

1994

Overview

The PA-7100LC was primarily designed as a single-chip solution for application in low cost systems while still delivering the performance of 1991 high-end workstations and servers. The CPU core design was leveraged from the PA-7100 and integrated with several of its off-chip support components on a single die. The PA-7100LC integrates the CPU, FPU, MIOC (*memory and I/O controller*) and a first-level cache on a single VLSI chip and has a direct attachment to the GSC main bus. Both CPU and FPU support the *PA-RISC 1.1 Edition 3 ISA*.

Details

- ◇ PA-RISC version 1.1c 32-bit
- ◇ Three functional units: 2 integer ALUs, 1 Floating Point unit (*See Note 1*)
- ◇ 2-way superscalar

¹⁰ http://www.hotchips.org/archives/hc4/2_Mon/HC4.S1/HC4.1.2.pdf

¹¹ http://www.hotchips.org/archives/hc4/2_Mon/HC4.S2/HC4.2.1.pdf

¹² <ftp://ftp.inria.fr/INRIA/publication/publi-pdf/RR/RR-3188.pdf>

- ◇ Not SMP-capable
- ◇ Five-stage pipeline
- ◇ DRAM memory & cache controller (MIOC) integrated on die, thus direct interface from the CPU to memory and cache
- ◇ 1KB on-chip I L1 instruction cache, direct mapped, 64-bit per access, prefetch from off-chip I cache
- ◇ 8KB-2MB off-chip unified I/D L1 cache, direct mapped, hashed address, virtual index, 480-600MB/s bandwidth
- ◇ The 1KB on-chip I cache is not really considered a true cache, thus the off-chip cache in fact is the system's real L1 cache
- ◇ 32-Byte cache line size
- ◇ Support for bi-endian load-store operations
- ◇ MAX-1 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Floating Point load-store to I/O space
- ◇ 64-entry unified I/D TLB, fully associative, 4K page size
- ◇ 8-entry BTLB, page sizes from 512K - 64M
- ◇ 64-bit wide load/store operations
- ◇ I and D cache bypassing
- ◇ *Stall on use* D cache miss policy
- ◇ *Don't fill on miss* cache hint
- ◇ Hardware TLB miss handler support
- ◇ Hardware *static* branch prediction
- ◇ GSC bus interface
- ◇ 64-bit ECC interface to the main memory
- ◇ Instruction line prefetch from main memory
- ◇ Up to 100MHz clock
- ◇ 14.2×14.2 mm² die, 900,000 FETs, 0.75μ(micron), 3-layer aluminium process packaged in a 432-pin PGA

Notes

1. Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition or multiplication. Both units can handle branch operations.

References

1. PA7100LC ERS (External Reference Specification)¹³ (.pdf) Hewlett-Packard Company (1999)
2. The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment¹⁴ Mick Bass et al (April 1995: Hewlett-Packard Journal. Accessed May 2009)
3. Design methodologies for the PA 7100LC microprocessor¹⁵ (.pdf) Mick Bass et al (April 1995: Hewlett-Packard Journal. Accessed May 2009)

2.2.7 PA-7200 (PCX-T') (*Thunderbird*)

Used in

- ◇ C100, C110
- ◇ D250, D260, D350, D360
- ◇ J200, J210
- ◇ K100, K200, K210, K220, K400, K410, K420
- ◇ Convex SPP1200/CD, SPP1200/XA, SPP1600/CD, SPP1600/XA
- ◇ Hitachi 9000V VQ200, VQ210, VR100, VR200, VR400

Time of introduction

Early 1995

Overview

The PA-7200 completely revised the PA-7100 processor core, leveraging only the FPU. Being a two-way superscalar processor, the PA-7200 can dispatch and execute two separate instructions at a time to its functional units. In contrast to the PA-7100 it has two separate integer ALUs and thus can execute two ALU integer operations simultaneously. Other changes include a redesigned cache architecture — while retaining the general cache layout with large off-chip L1 caches at CPU clock speed — and use of the Runway processor bus, carried on to later PA-8x00 processors. The PA-7200 was targeted towards high-performance general-purpose applications, but also on specialized applications with large working sets which could take advantage of the high-bandwidth bus interface.

Details

- ◇ PA-RISC version 1.1d 32-bit
- ◇ Three functional units: 2 integer ALUs, 1 Floating Point
- ◇ 2-way superscalar

¹³ http://ftp.parisc-linux.org/docs/chips/PCXL_ers.pdf

¹⁴ <http://www.hpl.hp.com/hpjournal/95apr/apr95a2.pdf>

¹⁵ <http://www.hpl.hp.com/hpjournal/95apr/apr95a3.pdf>

- ◇ SMP-capable
- ◇ FPU, MMU, cache controller integrated on die, memory and I/O controller separate and off-chip
- ◇ Five-stage pipeline
- ◇ 2KB on-chip “assist” L1 cache, fully associative, holds 64 32-Byte cache lines
- ◇ Off-chip L1 caches up to 1MB I and 2MB D realized in asynchronous SRAMs with one cycle latency
- ◇ (The 2KB on-chip *assist* cache is not really considered a true cache, thus the off-chip cache is the system’s L1 cache.)
- ◇ Caches are 64-bit per access, direct mapped, parity protected and cycled at CPU speed
- ◇ Caches are virtually indexed and physically tagged to minimize latency
- ◇ 120-entry fully associative TLB
- ◇ 16-entry BTLB
- ◇ Hardware TLB miss support
- ◇ Six predecode bits
- ◇ Support for uncached memory pages
- ◇ Bi-endian support
- ◇ Runway system interface, 64-bit wide, 120MHz, 960MB/s peak bandwidth, CPU-to-bus frequency ratios of 1.0, 0.75 and .67 processor speed possible
- ◇ Glueless interface to the Runway system bus for up to four-way SMP (four CPUs on same Runway processor bus)
- ◇ Can have up to six bus-transactions in progress at once
- ◇ CPU interfaces to U2 I/O adapters and MMC/SMC memory controllers on the Runway bus
- ◇ Up to 140MHz frequency with 4.4V core and 3.3V I/O voltage
- ◇ 14.0×15.0 mm² die, 1,300,000 FETs, 0.55μ(micron), 3-layer metal CMOS (CMOS14A process) packaged in a 540-pin ceramic PGA package
- ◇ Power dissipation of 29W at 140MHz

References

1. **Design of the HP PA 7200 CPU**¹⁶ (.pdf) Kenneth K. Chan et al (February 1996: Hewlett-Packard Journal)
2. **A Different Kind of RISC**¹⁷ Dick Pountain (August 1994: BYTE Journal)
3. Interview with David Fotland, September/October 2008

¹⁶ http://ftp.parisc-linux.org/docs/whitepapers/pa7200_design.pdf

¹⁷ <http://www.byte.com/art/9408/sec11/art3.htm>

2.2.8 PA-7300LC (PCX-L2) (*Velociraptor*)

Used in

- ◇ 744, 745, 748
- ◇ A180, A180C
- ◇ B132L, B132L+, B160L, B180L+
- ◇ C132L, C160L
- ◇ D220, D230, D320, D330
- ◇ RDI PrecisionBook
- ◇ Hitachi 3050RX 255, 355E, 365

Time of introduction

Mid 1996

Overview

The PA-7300LC is the direct descendant of the PA-7100LC and likewise designed for low-cost systems. It is still a PA-RISC 1.1 32-bit processor in contrast to the new PA-RISC 2.0 64-bit PA-8000 introduced in the same timeframe. While the PA-7300LC is rather close to the original PA-7100LC design it has several significant enhancements:

1. Large on-chip L1 caches, in contrast to the small “assist” caches of the 7100LC and 7200
2. Integrated L2 controller in the MIOC
3. Improved bus interface, a faster GSC

The then current process technologies made it possible to include a large L1 cache on the CPU die, breaking a long-standing HP tradition of large off-chip L1 caches. The PA-7300LC was the final 32-bit, PA-RISC version 1.1 CPU, later workstations and servers used 64-bit PA-RISC 2.0 processors.

- ◇ PA-RISC version 1.1e 32-bit
- ◇ Three functional units: 2 integer ALUs, 1 Floating Point unit (*See Note 1*)
- ◇ 2-way superscalar
- ◇ MAX-1 multimedia extensions (subword arithmetic) for multimedia applications (not explicitly mentioned on the PA7300LC, but its documentation states support for MAX-1 instructions)
- ◇ 64KB/64KB I/D on-chip L1 caches, each two-way set associative, virtually indexed
- ◇ Cache line size of 32 Byte
- ◇ Caches have a 64-bit datapath to the execution units, 256-bit datapath to main memory
- ◇ Optional unified I/D L2 off-chip cache, up to 8192KB
- ◇ No hashing for both I and D caches
- ◇ L2 cache is write-through, direct mapped, physically indexed and physically tagged

- ◇ Instruction prefetch buffer moved from memory controller to L1 instruction cache, thus allowing prefetch hits without penalty
- ◇ On-chip MIOC memory controller
- ◇ 96-entry unified I/D TLB
- ◇ 8-entry BTLB
- ◇ 4-entry ILAB
- ◇ GSC system interface (implements GSC+ features), maximum clock frequency of 40MHz — actual system implement from 33MHz (132MB/s), 36MHz (140MB/s) and up to 40MHz (160MB/s)
- ◇ Either 64-bit or 128-bit datapath from execution units to the memory
- ◇ Up to 180MHz frequency with 3.3V core voltage
- ◇ 15.3×17.0 mm² die, 9,200,000 FETs, 0.5μ(micron), 4-layer metal CMOS (CMOS14C process) packaged in a 464-pin ceramic PGA package

Notes

1. Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition or multiplication. Both units can handle branch operations.

References

- ◇ PA7300LC ERS (External Reference Specification)¹⁸ (PDF, 716KB) Hewlett-Packard Company (1996).
- ◇ The PA-7300LC: the first “System on a Chip”¹⁹ (archive.org mirror) Tom Meyer (1996: Presentation for Microprocessor Forum 1995).
- ◇ The PA 7300LC Microprocessor: A Highly Integrated System on a Chip²⁰ (PDF, 50KB). Terry W. Blanchard and Paul G. Tobin (June 1997: Hewlett-Packard Journal).

2.2.9 PA-8000 (PCX-U) (*Onyx*)

Used in

- ◇ C160, C180
- ◇ D270, D280, D370, D380
- ◇ J280, J282
- ◇ K250, K260, K450, K460
- ◇ R380
- ◇ T600
- ◇ HP/Convex SPP2000 (S-Class/X-Class)

¹⁸ http://ftp.parisc-linux.org/docs/chips/pcxl2_ers.pdf

¹⁹ http://web.archive.org/web/20040214111649/http://www.cpus.hp.com/technical_references/101995wp.shtml

²⁰ http://ftp.parisc-linux.org/docs/whitepapers/pa7300lc_on_chip.pdf

◇ Stratus Continuum 628, 1228

Time of introduction

January 1996

Overview

The PA-8000 is a four-way superscalar 64-bit processor with aggressive out-of-order (*OoO*) execution capabilities. It has four integer, four floating-point and dual load/store units, a large *OoO* dispatch window and, following a long HP tradition, no on-chip caches. The PA-8000 is the first chip to implement the 64-bit PA-RISC 2.0 architecture which includes many extensions to support 64-bit computing. This includes that all integer registers and functional units (ALU, shift/merge) have been widened to 64-bit to support native 64-bit integer computing. The flat address space was also extended from 32- to 64-bit —however, PA-RISC 2.0 processors support only a physical address space/addressable physical memory of 40-bit/1TB (PA-8000 to PA-8600) to 44-bit/16TB (PA-8700 and up). Other extensions in the PA-8000 include fast TLB insert instructions, memory prefetch instructions, support for variable sized pages, branch prediction hinting and new FPMAC (*Floating Point Multiply Accumulate*) units. The instruction decode logic is not integrated with the functional units' pipeline logic, which allows the chip to partially decode instructions in advance of the actual execution (by the functional units).

A key feature of the PA-8000 and all other PA-RISC 2.0 processors is the IRB (*Instruction Reorder Buffer*), which enables the processor to perform its own instruction scheduling in hardware, independent of compiler or other software technologies. The IRB can store up to 28 computation and 28 load/store instructions; it tracks interdependencies between these instructions and allows execution as soon as they are ready. Also tracked are branch prediction outcomes and with re-scheduling the CPU can execute instructions past cache misses. The IRB plays the key part in the *OoO* execution capability of the chip.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ Two address adders
- ◇ 96-entry fully-associative dual-ported TLB
- ◇ TLB miss penalty of 61 cycles
- ◇ 32-entry BTAC (*Branch Target Address Cache*)
- ◇ 256-entry BHT (*Branch History Table*)
- ◇ *Dynamic* and *static* branch prediction modes

- ◇ Off-chip L1 caches up to 1MB I and 1MB D, realized in synchronous 6.7ns (150MHz) late-write 1Mb SRAMs, one cycle latency
- ◇ Caches are direct-mapped and dual-ported
- ◇ 56-entry instruction queue/reorder buffer (*IRB*)
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Each instruction includes five predecode bits
- ◇ Bi-endian support
- ◇ Runway system/memory bus, 120MHz, 64-bit wide, featuring split transactions and glueless multiprocessing. Max. throughput of 960MB/s
- ◇ CPU interfaces to UTurn I/O adapters and MMC/SMC memory controllers on the Runway bus
- ◇ Up to 180MHz frequency with 3.3V core voltage
- ◇ 17.7×19.6 mm² die, 4,500,000 FETs, 0.5μ(micron), 5-layer metal CMOS packaged in a 1,085-pin flip-chip LGA package

References

- ◇ **Advanced Performance features of the 64-bit PA-8000**²¹ (archive.org mirror) Doug Hunt (1995: IEEE CS Press CompCon 5). [Article reprint for cpus.hp.com]
- ◇ **PA-8000 Combines Complexity and Speed**²² (archive.org mirror) Linley Gwennap (1994: Micro-processor Report, Volume 8 Number 15). [Article reprint for vanished cpus.hp.com]
- ◇ **Four-Way Superscalar PA-RISC Processors**²³ (PDF, 190KB) Anne P. Scott et al (August 1997: Hewlett-Packard Journal).

2.2.10 PA-8200 (PCX-U+) (*Vulcan*)

Used in

- ◇ C200, C240
- ◇ D390
- ◇ J2240
- ◇ K370, K380, K570, K580
- ◇ R390
- ◇ V2200, V2250

²¹ http://web.archive.org/web/20040214092531/http://www.cpus.hp.com/technical_references/advperf.shtml

²² http://web.archive.org/web/20040214122429/http://www.cpus.hp.com/technical_references/111994ar.shtml

²³ http://ftp.parisc-linux.org/docs/whitepapers/four_way_superscalar.pdf

Time of introduction

May 1997

Overview

Shortly after the introduction of the PA-8000 the design team noted several aspects of this chip for improvement in the successor:

- ◇ Branch prediction
- ◇ TLB miss rates
- ◇ Cache sizes

The new chip should offer improved performance, compatibility with existing applications and short time to market, with the whole design heavily leveraged from the existing PA-8000 foundation. The availability of new 4Mb SRAMs with faster access times allowed for an increased CPU clock speed and bigger caches. Smaller changes include an increase to the BHT and TLB as “high benefit, low risk” improvements.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ Two address adders
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 120-entry fully-associative dual-ported TLB
- ◇ 42-entry BTAC (*Branch Target Address Cache*)
- ◇ 1024-entry BHT (*Branch History Table*)
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ Off-chip L1 caches up to 2MB I and 2MB D, realized in synchronous 5ns (200MHz) late-write 4Mb SRAMs, one cycle latency
- ◇ Caches are direct-mapped and dual-ported
- ◇ 56-entry instruction queue/reorder buffer (*IRB*)
- ◇ Each instruction includes five predecode bits
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Bi-endian support

- ◇ Runway system/memory bus, 120MHz, 64-bit wide, featuring split transactions and glueless multiprocessing. Max. throughput of 960MB/s
- ◇ CPU interfaces to UTurn I/O adapters and MMC/SMC memory controllers on the Runway bus
- ◇ Up to 300MHz frequency with 3.3V core voltage
- ◇ 17.7×19.6 mm² die, 4,500,000 FETs, 0.5μ(micron), 5-layer metal CMOS packaged in a 1,085-pin flip-chip LGA package

References

- ◇ **Four-Way Superscalar PA-RISC Processors**²⁴ (PDF, 190KB) Anne P. Scott et al (August 1997: Hewlett-Packard Journal).
- ◇ **HP Pumps Up PA-8x00 Family**²⁵ (archive.org mirror) Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for vanished cpu.hp.com]

2.2.11 PA-8500 (PCX-W) (*Vulcan*)

Used in

- ◇ A400-44 (rp2400), A500-44 (rp2450)
- ◇ B1000, B2000
- ◇ C360, C3000
- ◇ J5000, J7000
- ◇ L1000-36, L1000-44 (rp5400), L2000-36, L2000-44 (rp5450)
- ◇ N4000-36, N4000-44 (rp7400)
- ◇ V2500
- ◇ Stratus Continuum 419, 429, 616S, 616, 619, 629, 1219, 1229

Time of introduction

September 1998

Overview

The PA-8500 processor is a direct evolution of the PA-8000 and PA-8200 processors, taking over a very similar processing core. However, the PA-8500 implemented large on-die L1 caches, a first for PA-RISC processors and a break with the long-standing HP tradition of keeping the large L1 caches off-chip. (The two years older PA-7300LC also includes on-chip L1 caches, albeit much smaller). There were no other significant changes to the processing core, besides small increases to the TLB and BHT.

²⁴ http://ftp.parisc-linux.org/docs/whitepapers/four_way_superscalar.pdf

²⁵ http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml

The main challenge in the PA-8500 development were the large on-chip L1 caches, which had to fit onto the allocated die area and be able to keep up with the instruction reordering in the IRB. The data cache is composed of 0.5MB banks, implemented with four 0.125MB arrays providing error correction. The instruction cache is implemented as one bank of 0.5MB four-way set associative pipelined cache, providing 128 bits of instruction per cycle plus pre-decode bits.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ Two address adders
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 160-entry fully-associative dual-ported TLB
- ◇ 32-entry BTAC (*branch target address cache*)
- ◇ 2048-entry BHT (*branch history table*)
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ On-chip L1 caches 0.5MB I and 1MB D, each 4-way set associative
- ◇ 32 or 64 Byte cache line size
- ◇ Supports up to 1 TB of physically addressable memory (40-bit physical addresses)
- ◇ 56-entry instruction queue/reorder buffer (*IRB*)
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Bi-endian support
- ◇ Runway+/Runway DDR system/memory bus, 125MHz, 64-bit, DDR (*double data rate*), about 2.0GB/s peak bandwidth
- ◇ CPU interfaces in most systems to the Astro memory and I/O controller (on very few configurations the PA-8500 attaches to the *DEW Runway ports/converters* of the Stretch chipset)
- ◇ Up to 440MHz frequency with 2.0V core voltage
- ◇ 21.3×22.0 mm² die, 140,000,000 FETs, 0.25μ(micron), 5-layer metal CMOS packaged in a 544-pin LGA package

References

- ◇ **HP Pumps Up PA-8x00 Family**²⁶ (archive.org mirror) Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for vanished [cpu.hp.com](http://www.cpu.hp.com)]

²⁶ http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml

- ◇ A 500 MHz 1.5 MByte Cache with On-Chip CPU²⁷ (PDF, 141KB) Jonathan Lachman and J. Michael Hill (1997: ISSCC).
- ◇ PA-8500: The Continuing Evolution of the PA-8000 Family²⁸ (archive.org mirror) Gregg Lesartre and Doug Hunt (1997: Proceedings of CompCon, IEEE CS Press). [Article reprint for vanished cpu.hp.com]

2.2.12 PA-8600 (PCX-W+) (*Landshark*)

Used in

- ◇ A400-5X (rp2400), A500-5X (rp2450)
- ◇ B2000 (some), B2600
- ◇ C3600
- ◇ J5600, J6000, J7600
- ◇ L1000-5X (rp5400), L2000-5X (rp5450)
- ◇ L1500-5X (rp5430), L3000-5X (rp5470)
- ◇ N4000-5X (rp7400)
- ◇ V2600
- ◇ Superdome
- ◇ Stratus Continuum 439, 449, 651-2, 652-2, 1251-2, 1252-2

Time of introduction

January 2000

Overview

The PA-8600 is a PA-8500 with minor modifications for a new manufacturing process in order to achieve higher clock speeds, which was the main aim of developing the PA-8600. One of the few changes to the original design is a *quasi LRU replacement* policy for the instruction cache.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ Two address adders

²⁷ http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk.pdf

²⁸ http://web.archive.org/web/20040214131135/http://www.cpus.hp.com/technical_references/8500.shtml

- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 160-entry fully-associative dual-ported TLB
- ◇ 32-entry BTAC (*branch target address cache*)
- ◇ 2048-entry BHT (*branch history table*)
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ On-chip L1 caches 0.5MB I and 1MB D, each 4-way set associative
- ◇ 32 or 64 Byte cache line size
- ◇ Supports up to 1 TB of physically addressable memory (40-bit physical addresses)
- ◇ 56-entry instruction queue/reorder buffer (*IRB*)
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Quasi LRU replacement policy for the instruction cache
- ◇ Bi-endian support
- ◇ Runway+/Runway DDR system/memory bus, 125MHz, 64-bit, DDR (*double data rate*), about 2.0GB/s peak bandwidth
- ◇ CPU interfaces in smaller systems to the Astro memory and I/O controller, in larger/mainframe systems to the *DEW Runway ports/converters* of the Stretch chipset or to the Cell chipset (probably with converters, since Cell is also an Itanium chipset)
- ◇ Up to about 550MHz frequency with 2.0V core voltage
- ◇ 21.3×22.0 mm² die, 140,000,000 FETs, 0.25μ(micron), 5-layer metal CMOS packaged in a 544-pin LGA package

2.2.13 PA-8700 (PCX-W2) (*Piranha*)

Used in

- ◇ A400-6X (rp2430), A500-6X, A500-7X (rp2470)
- ◇ C3650, C3700, C3750
- ◇ J6700
- ◇ L1500-6X, L1500-7X, L1500-8X (rp5430), L3000-6X, L3000-7X, L3000-8X (rp5470)
- ◇ N4000-6X, N4000-7X (rp7400)
- ◇ N4000-6X, N4000-7X, N4000-8X (rp7405, rp7410)
- ◇ Superdome

Time of introduction

August 2001

Overview

The PA-8700 is an enhanced PA-8500 core with several modifications. As all PA-8x00 processors the PA-8000, the logic core is still very close to the original PA-8000 core from 1997. All subsequent PA-RISC processors from HP were based on this basic PA-RISC version 2.0 design while adding features and slight modification. The PA-8700 significantly enhanced the on-chip L1 caches and TLB while switching to a new manufacturing process helped increasing the clock speed. The PA-8700 was at its time one of the largest available commercial processors and one of the first manufactured in a SOI (Silicon On Insulator) process. After the Intel-fabbed PA-8500 and PA-8600, the PA-8700 was produced in IBM's fabs after HP gave up its own in the 1990s.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ Two address adders
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 240-entry fully-associative dual-ported TLB
- ◇ 32-entry BTAC (*branch target address cache*)
- ◇ 2048-entry BHT (*branch history table*)
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ 0.75MB I and 1.5MB D on-chip L1 caches, each 4-way set associative, implemented in independent 0.75MB banks.
- ◇ 32 or 64 Byte cache line size
- ◇ Data cache prefetching
- ◇ Quasi LRU replacement policy for *both* the instruction and data cache.
- ◇ Supports up to 16 TB of physically addressable memory (44-bit physical addresses)
- ◇ 56-entry instruction queue/reorder buffer (*IRB*)
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ Bi-endian support
- ◇ Support for hardware lock-stepping, i.e. operating multiple chips in parallel to detect faults
- ◇ Runway+/Runway DDR system/memory bus, 125MHz, 64-bit, DDR (*double data rate*), about 2.0GB/s peak bandwidth
- ◇ CPU interfaces in smaller systems to the Astro memory and I/O controller, in larger/mainframe systems to the *DEW Runway ports/converters* of the Stretch chipset or to the Cell chipset (probably with converters, since Cell is also an Itanium chipset)

- ◇ Up to 750MHz (875MHz on the PA-8700+) frequency with 1.5V core voltage
- ◇ 16.0×19.0 mm² die, 186,000,000 FETs, 0.18μ(micron), 7-layer Silicon-on-Insulator CMOS packaged in a 544-pin LGA package

References

- ◇ **A 900MHz 2.25MByte Cache with On Chip CPU**²⁹ (PDF, 119KB) J. Michael Hill and Jonathan Lachman (2000: ISSCC).

2.2.14 PA-8800 (*Mako*)

Used in

- ◇ C8000
- ◇ L1500-9X (rp5430), L2000-9X (rp5450)
- ◇ N4000-9X (rp7405, rp7410)
- ◇ rp3410, rp3440
- ◇ rp4410, rp4440
- ◇ rp7420
- ◇ rp8400, rp8410, rp8420
- ◇ Superdome

Time of introduction

2004

Overview

The dual-core PA-8800 *Mako* consists of two separate PA-8700 cores on a single die with very large off-die L2 caches on the processor module. The clock speed was only increased slightly, while the processor bus interface was redesigned to use the HP/Intel Itanium/McKinley bus. *Mako* was supposed to breathe fresh life in the PA-RISC line, though it had strong internal competition from the **Itanium**³⁰ line, based on HP development together with **Intel**³¹, and was not marketed much. Most systems supporting PA-8800s use the HP zx1 chipset and could be hardware-upgraded to use Itanium 2/IA64 processors.

²⁹ http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk_2.pdf

³⁰ <http://en.wikipedia.org/wiki/Itanium>

³¹ <http://www.intel.com>

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Twenty functional units: four integer ALUs, four shift/merge units, four complete load/store pipelines, four Floating Point multiply/accumulate units, four Floating Point divide/square root units
- ◇ 4-way superscalar
- ◇ Two address adders
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 240-entry fully-associative dual-ported TLB per core
- ◇ 32-entry BTAC (*branch target address cache*) per core
- ◇ 2048-entry BHT (*branch history table*) per core
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ 0.75MB I and 0.75MB D on-chip L1 caches *per core*
- ◇ No data passing between the cores' L1 caches
- ◇ 32MB off-chip L2 cache, four-way associative, physically indexed and tagged
- ◇ L2 cache is shared between both CPU cores
- ◇ L2 cache controller is on-die
- ◇ L2 implemented in DDR-ESRAM, four 8MB chips, 300MHz clock, each 2.7GB/s bandwidth
- ◇ Total >10GB/s L2 cache bandwidth
- ◇ 1MB SRAM tags for L2 cache
- ◇ ECC for L2 data and tags
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ *Itanium 2/McKinley* processor bus, 200MHz clock (“double-pumped”), 128-bit datapath, 6.4GB/s bandwidth, data ECC-protected, signals parity
- ◇ CPU interfaces to the Cell chipset or the zxi chipset's MIO
- ◇ Up to 1 GHz frequency with 1.5V core voltage
- ◇ 23.6×15.5 mm² die, 300,000,000 FETs, 0.13μ(micron), 8-layer Silicon-on-Insulator CMOS (fabbed by IBM)

References

- ◇ **HP's Mako Processor**³² (PDF, 1.4MB) David J. C. Johnson (2001: Microprocessor Forum).

³² http://ftp.parisc-linux.org/docs/whitepapers/mako_mpf_2001.pdf

2.2.15 PA-8900

Used in

- ◇ rp3410, rp3440
- ◇ rp4410, rp4440
- ◇ rp7440, rp8440
- ◇ C8000
- ◇ L1500-9X (rp5430), L2000-9X (rp5450) (probably)
- ◇ N4000-9X (rp7405, rp7410) (probably)
- ◇ Superdome

Time of introduction

2005

Overview

The PA-8900 is a slightly tweaked PA-8800 processor with a doubled L2 cache and higher clock frequency, keeping the tradition of only small upgrades in the 64-bit processor generation. It is probably the last processor of the PA-RISC family. Future systems will be based on Itanium-family chips. After HP dropped its line of Itanium *workstations* the PA-8900-powered C8000 workstation re one of the last HP-UX workstations.

Information on the PA-8900 is limited, it seems there was not much interest releasing details on its architecture.

Details

- ◇ PA-RISC version 2.0 64-bit
- ◇ Twenty functional units: four integer ALUs, four shift/merge units, four complete load/store pipelines, four Floating Point multiply/accumulate units, four Floating Point divide/square root units
- ◇ Two address adders
- ◇ SMP-capable
- ◇ External memory and I/O controllers
- ◇ 240-entry fully-associative dual-ported TLB per core
- ◇ 32-entry BTAC (*branch target address cache*) per core
- ◇ 2048-entry BHT (*branch history table*) per core
- ◇ *Dynamic* and *static* branch prediction modes
- ◇ 4-way superscalar

- ◇ 0.75MB I and 0.75MB D on-chip L1 caches *per core*
- ◇ 64MB off-chip L2 cache, four-way associative, physically indexed and tagged
- ◇ ECC for L2 data and tags
- ◇ MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ *Itanium 2/McKinley* processor bus, 200MHz clock (“double-pumped”), 128-bit datapath, 6.4GB/s bandwidth, data ECC-protected, signals parity
- ◇ CPU interfaces to the Cell chipset or the zx1 chipset’s MIO
- ◇ 44 bit physical addressing
- ◇ 64 bit virtual addressing
- ◇ Four GB maximum page size
- ◇ Up to 1.1 GHz frequency
- ◇ 23.6×15.5 mm² die, 317,000,000 FETs, 0.13μ(micron), 8-layer Silicon-on-Insulator CMOS (apparently fabbed by IBM)

References

- ◇ Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers³³ (PDF, 700KB) Hewlett-Packard (2005).

2.2.16 Hitachi PA/50

Used in

- ◇ Hitachi 3050RX 100C, 200

Time of introduction

About 1993

Overview

The PA/50 is a PA-RISC version 1.1 compatible processor designed and manufactured by Hitachi. Two designs were developed: M and L (L for low-cost). They were used as personal workstation processors and high-end embedded controllers. Hitachi integrated a set of features previously not implemented at that time in other PA-RISC processors, *e.g.*, on-chip caches, data-prefetching, a power-saving mode and SDRAM support.

³³ <http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf>

Details

- ◇ PA-RISC version 1.1 32-bit
- ◇ Built-in, pipelined FPU
- ◇ L1 I: 8KB, 2-way set-associative, 32-byte blocks
- ◇ L1 D: 4KB, 2-way set-associative, 32-byte blocks, copy-back
- ◇ L1 caches are on-chip
- ◇ Uncacheable memory (per page)
- ◇ TLB: I/D 32/64-entry, 2-way set, 4K-page, each +2 additional block entries
- ◇ BTLB (256KB-32MB)
- ◇ Seven 32-bit shadow registers for fast interrupts
- ◇ Data-prefetching
- ◇ Non-blocking cache
- ◇ Power-saving mode, reducing frequency to 1/8
- ◇ Support for SDRAM
- ◇ PA/50L: Up to 33MHz frequency with 3.3V core voltage
- ◇ PA/50M: Up to 60MHz frequency with 5.0V core voltage
- ◇ 11.5×12.0 mm² die, 1,280,000 FETs, 0.6μ(micron), 3-layer metal CMOS packaged in a 160-pin plastic QFP package

References

- ◇ **PROgress (PA-RISC) Newsletter - comp.sys.hp**³⁴ Candace Doyle (October 1993: Precision Risc Organization. Accessed December 2007)

2.2.17 Hitachi HARP-1**Used in**

- ◇ Hitachi SR2201 supercomputer (HARP-1E)
- ◇ Probably others

Time of introduction

June 1994

³⁴ <http://groups.google.com/group/comp.sys.hp/msg/32de7bed6bae1c42>

Overview

The HARP-1 is a PA-RISC version 1.1 compatible CPU from Hitachi, apparently a larger and faster version of the above PA/50. Not much information is available on the processors.

Apparently the HARP-1E variant includes (“pseudo”) vector processing modifications/add-ons and was used in Hitachi vector/supercomputers. It seems the L1 cache was increased to 16KB/16KB instruction/data.

Details

- ◇ PA-RISC version 1.1 32-bit
- ◇ Three functional units: two integer ALUs and one floating point unit (and two shift-merge units)
- ◇ Six-stage pipeline
- ◇ Built-in, pipelined FPU
- ◇ Built-in memory controller (Memory Interface Unit, MIU)
- ◇ 2-way superscalar
- ◇ L1 I cache: 8KB, 1-way set-associative, 32-byte blocks
- ◇ L1 D cache: 16KB, 2-way set-associative, 32-byte blocks, copy-back
- ◇ L1 caches are on-chip
- ◇ L2 I/D 512/512KB, off-chip
- ◇ TLB: I/D 128/128-entry, 1-way set
- ◇ (Some say a second level TLB was included)
- ◇ L2 Cache bus: 128-bit (ECC) data path to L2 caches
- ◇ Processor bus: 64-bit (parity) data path to main memory and I/O
- ◇ Up to 150MHz frequency with 3.3V core voltage, 17W power dissipation (at 120MHz)
- ◇ 16.2×16.5 mm² die, 2,800,000 FETs, 0.5μ(micron) 3-layer aluminium + 1-layer tungsten BiC-MOS, packaged in 595-pin PGA

References

1. **Chronology of Workstation Computers (1993)**³⁵ Ken Polsson (November 2007. Accessed November 2007)
2. **PROgress (PA-RISC) Newsletter - comp.sys.hp**³⁶ Candace Doyle (October 1993: Precision Risc Organization. Accessed December 2007)
3. **Basic Concept of Cooperative Timing-driven Design Automation Technology for High-speed RISC Processor HARP-1**³⁷ (PDF) Hidekazu Terai et al (October 1999: Hitachi Ltd. Accessed January 2008)

³⁵ <http://www.islandnet.com/~kpolsson/workstat/work1993.htm>

³⁶ <http://groups.google.com/group/comp.sys.hp/msg/32de7bed6bae1c42>

³⁷ http://www.sigda.org/Archives/ProceedingArchives/Dac/Dac94/papers/1994/dac94/pdffiles/17_3.pdf

4. *A 120-MHz BiCMOS Superscalar RISC Processor*, Shigeya Tanaka et al (IEEE Journal of Solid-State Circuits, vol. 29, no. 4, April 1994)

2.2.18 Other processors

Table 2.2: Other PA-RISC processors overview

CPU	ISA	Clock max	FETs	Cache	Bus	Super scalar	Units	Controllers on-chip
Winbond W89K	PA 1.1 32-bit	33/66MHz	1.1M	2/2KB I/D on-chip L1	Intel 486	1-way	1 Integer	none?
Winbond W90210 W90215	PA 1.1 32-bit	33/66MHz	?	4/8KB I/D on-chip L1	Intel 486	1-way	1 Integer MAX-1	DRAM DMA PCI I/O
Winbond W90220 W90221	PA 1.1 32-bit	150MHz	?	4/4KB I/D on-chip L1	Intel 486	1-way	1 Integer 1 MAC(DSP) MAX-1	DRAM DMA PCI IDE I/O VGA (W90221) TV (W90221)
Oki OP32	PA 1.1 32-bit	33MHz	1.1M	?	?	1-way	1 Integer	DRAM DMA

Winbond W89K

Time of introduction: Spring 1994

The Winbond W89K is an embedded 32-bit PA-RISC controller chip, pin-compatible with the then-popular Intel 80486DX. It could be used as a drop-in replacement in mid-1990s PCs together with Winbond BIOS replacement chips. Rationale was to allow hardware developers utilize existing 486DX mainboards and components for a shorter product development process. The W89K is a *level 0* PA-RISC 1.1 implementation: a 32-bit PA-RISC processor without virtual addressing.

- ✧ PA-RISC version 1.1 (third edition) 32-bit
- ✧ Level 0 implementation (no virtual addressing): no MMU
- ✧ Five-stage pipeline
- ✧ One functional unit: one 32-bit integer ALU
- ✧ 2KB/2KB I/D on-chip L1 caches
- ✧ 80486 (Intel) bus interface
- ✧ 33MHz and 66MHz clock speeds were available, with the latter apparently having been achieved with a clock-doubling also used in the Intel's 80486DX/2 (the chips uses an internal clock-doubler on the external 33MHz bus)
- ✧ On-chip JTAG support
- ✧ 14.3×14.3 mm² die, 1,100,000 FETs, 0.8μ(micron), 3-layer metal CMOS

References

- ◇ **PROgress (PA-RISC) Newsletter - comp.sys.hp**³⁸ Candace Doyle (October 1993: Precision Risc Organization. Accessed December 2007)
- ◇ **Winbond, Varian sign deal for thin-film IC process**³⁹ Terho Uimonen (April 1994: Electronic News. Accessed January 2008 at findarticles.com)
- ◇ **PA-RISC in a PC box (was: Re: HP's vision of a low-end 3000) - comp.sys.hp.mpe**⁴⁰ Stan Sieler (Februar 1996. Accessed December 2007)

Winbond W90210/215

Time of introduction: Fall 1997

Shortly after the W89K embedded controllers Winbond introduced more sophisticated PA-RISC processors with the W90K line of embedded controllers. The W90210F still was 32-bit PA-RISC 1.1 but integrated many external I/O components on the chip — DRAM and DMA controllers, a PCI bridge and various I/O ports. As its predecessor, the W90210F was a level 0 PA-RISC 1.1 implementation without virtual addressing. It was apparently used in various “Internet appliances”: set-top boxes, TV sets, DVD players, PDAs, VoIP devices, and for industrial automation. The W90215 is identical to the W90210 but did not include license rights for the embedded operating system (and was thus cheaper).

- ◇ PA-RISC version 1.1 (third edition) 32-bit
- ◇ Level 0 implementation (no virtual addressing): no MMU
- ◇ Five-stage pipeline
- ◇ One functional unit: one 32-bit integer ALU
- ◇ L1 I cache: 4KB, direct mapped, 32-byte blocks, 256 entries
- ◇ L1 D cache: 8KB, 2-way set-associative, 32-byte blocks, 2×64 entries, write-back
- ◇ MAX-1 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ 80486 (Intel) bus interface
- ◇ DRAM controller
- ◇ ROM/FLASH interface
- ◇ DMA controller (2-channel 8-bit)
- ◇ PCI bridge
- ◇ Two serial ports
- ◇ Parallel port
- ◇ 33MHz and 66MHz clock speeds (?)
- ◇ 208-pin PQF package

References

³⁸ <http://groups.google.com/group/comp.sys.hp/msg/32de7bed6bae1c42>

³⁹ http://findarticles.com/p/articles/mi_m0EKF/is_n2011_v40/ai_15334690

⁴⁰ <http://groups.google.com/group/comp.sys.hp.mpe/msg/3a30of81ddfd151>

- ◇ **W90210F PA-RISC Embedded Controller**⁴¹ (.pdf) Winbond Electronics Corp. (October 1997. Accessed January 2008)

Winbond W90220 and W90221

Time of introduction: Spring 1999

The W90220F is, as its predecessor W90210, a 32-bit PA-RISC 1.1 design without MMU but integrated many external I/O components on the chip — DRAM and DMA controllers, PCI bridge, IDE channels, I/O ports and, on the W90221, a graphics/TV chip. It had the same target systems of set-top boxes and internet appliances. The successor W90221 is apparently similar, with higher clock speed, integrated (S)VGA and TV controller

- ◇ PA-RISC version 1.1 (third edition) 32-bit
- ◇ Level 0 implementation (no virtual addressing): no MMU
- ◇ Six-stage pipeline
- ◇ Two functional units: one 32-bit integer ALU and one 32-bit multiply-accumulate (MAC) module (for DSP purposes, can be used as two 16-bit modules too)
- ◇ L1 I cache: 4KB, direct mapped, 32-byte blocks, 256 entries
- ◇ L1 D cache: 4KB, 4-way set-associative, write-back or write-through
- ◇ MAX-1 multimedia extensions (subword arithmetic) for multimedia applications, *e.g.*, MPEG decoding
- ◇ 80486 (Intel) bus interface
- ◇ Hardware *dynamic* branch prediction
- ◇ 256-entry branch-target-buffer (i. e. BTAC)
- ◇ Memory controller (supports DRAM, EDO-DRAM and SRAM; W90221 additionally SDRAM)
- ◇ ROM/FLASH interface
- ◇ DMA controller (2-channel 8-bit)
- ◇ IDE I/O controller (four 16-bit channels)
- ◇ W90221: VGA and TV controller (W9971)
- ◇ PCI bridge
- ◇ Two serial ports
- ◇ Parallel port
- ◇ Serial ICE port
- ◇ Up to 150MHz clock speed at 3.3V/5V I/O and 3.3V core
- ◇ W90221: 133MHz clock speed with apparently 3.3V at both I/O and core
- ◇ 0.35μ(micron) single-poly-triple-metal CMOS
- ◇ 208-pin PQF package

⁴¹ <http://www.datasheetarchive.com/pdf/3656144.pdf>

References

- ◇ **W90220F PA-RISC Embedded Controller**⁴² (.pdf) Winbond Electronics Corp. (March 1999. Accessed January 2008)

Oki OP32

Oki Semiconductor OP32/50N was introduced in 1994 as an embedded controller, based on a 32-bit PA-RISC design with integrated DRAM and DMA controllers. The chip was targeted at laser printers, Fax machines, X-Terminals and the Telecom and Automotive markets.

- ◇ PA-RISC version 1.1 32-bit
- ◇ 33MHz frequency
- ◇ 14.3×14.3 mm² die, 1,100,000 FETs, 0.8μ(micron), 3-layer metal CMOS

References

- ◇ **PROgress (PA-RISC) Newsletter - comp.sys.hp**⁴³ Candace Doyle (October 1993: Precision Risc Organization. Accessed December 2007)

⁴² <http://www.datasheetarchive.com/pdf/3656145.pdf>

⁴³ <http://groups.google.com/group/comp.sys.hp/msg/32de7bed6bae1c42>

2.3 PA-RISC CPU Architecture

2.3.1 PA-RISC overview

PA-RISC was HP's take on RISC and the 1980s offspring of previous design efforts and lessons that HP⁴⁴ learned from developing the FOCUS CPU. The PA-RISC processors were designed to replace the 16-bit stack-based CPUs in HP 3000 servers and Motorola 680x0 CPUs in HP's Unix systems, and unify all commercial products onto a common system architecture. At the time of development RISC (Reduced Instruction Set Computing) platforms were largely expected to replace the CISC architectures, with well known examples as Intel x86, Motorola 68k.

Overall PA-RISC was a rather conservative RISC design:

- ✧ The instruction set is implemented in hardware and not microcoded, as for in example in conventional CISCs (or HP FOCUS).
- ✧ The instruction size has a fixed length — one word (32-bit).
- ✧ Only three addressing modes: long/short displacement and indexed mode.
- ✧ Only load/store operation access the memory, no computational instructions directly access the memory.
- ✧ The PA-RISC instruction set was designed to be a good target for optimizing compilers. Many simple, frequently used instructions execute in just one cycle, more complex computation were assigned to assist processors or software algorithms.

Compared to other RISC architectures from the time the original PA-RISC design was rather unspectacular — it had typically fewer features but remained always at competitive speeds, especially in Floating Point and SMP (multiprocessing) areas. HP was the first to include multimedia extension in a commercially available microprocessor (MAX-1 in the PA-7100LC and MAX-2 64-bit in the PA-8000 — similar to Intel's MMX et al.) which allowed vector operations on two or four 16-bit subwords in 32-bit or 64-bit integer registers.

The original PA-RISC 1.0 architecture included a single instruction/data bus; PA-RISC later on moved to a Harvard-style architecture with separate instruction and data buses. It has thirty-two 32-bit integer general purpose registers (GR0-GR31), seven shadow registers (SR0-SR6) for fast-interrupts and thirty-two 64-bit Floating Point registers for the FPU, which also could be combined to 64×32-bit and 16×128-bit. The FPU is able to execute a Floating Point instruction simultaneously to the ALU. The original addressing was 48-bit wide, it was later on expanded to 64-bit (with the introduction of the PA-8000 line). (*See Note 1*)

The PA-RISC architecture was extended to version 1.1 with the PA-7000 processor in 1991. The major change in PA-RISC 1.1 was the inclusion of a MMU (memory management unit), that enables the PA-RISC platform to use virtual memory. From the the second PA-RISC 1.1 processor, the PA-7100, onward all processors implement superscalar instruction execution — the ability to execute multiple instructions simultaneously. The 32-bit variants are up to two-way superscalar, later 64-bit processors up to four-way. Other significant developments include the PA-7100LC and PA-7300LC (LC for low cost) processors, which integrate the memory and I/O controller onto the processor die (on the PA-7300LC additionally the cache controller and first-level cache).

In 1996 the 64-bit redesign of the PA-RISC architecture was introduced with the PA-RISC 2.0 PA-8000 processor. The architectural changes were rather intrusive, while staying compatible with the

⁴⁴ <http://www.hp.com>

32-bit PA-RISC 1.1. (On a sidenote, the PA-8000 was introduced *before* the last 32-bit processor—the PA-7300LC—shipped.) Main changes in PA-RISC 2.0 include:

- ✧ All registers and functional units have been extended to 64-bit
- ✧ Virtual address space is 64-bit
- ✧ Physical address space is 40-bit on PA-8000 to PA-8600 (1TB of addressable physical memory) and 44-bit (16TB memory) on PA-8700 and later
- ✧ Out-of-Order (OoO) execution capability with the IRB (*Instruction Reorder Buffer*), which stores up to 28 computation and 28 load/store instructions and reorders and prepares the for execution on the fly. It tracks interdependencies and branch prediction outcomes as well. The IRB is *the* key part in the OoO execution capability of PA-RISC 2.0.
- ✧ FPMAC (*Floating Point Multiply Accumulate*) units

The later PA-8x00 processors did not introduce other significant changes besides higher integration, such as large L1 caches in the PA-8600 and the dual-core PA-8800 and PA-8900. In fact all processors after the PA-8000 were only redesigns and extensions of that processor core.

From the mid-1990s on a parallel track to PA-RISC 2.0 development HP joined Intel in developing the VLIW Itanium architecture from its own R&D projects (called EPIC), which resulted in the Intel/HP IA64 architecture. Since the early-2000s HP sold two lines of Unix computers and servers in parallel—both PA-RISC 2.0 and Itanium.

Notes

1. Great Microprocessors of the Past and Present⁴⁵, John Bayko (June 2001/V 12.1.1: BURKS. Accessed 28 Dec 2007)

2.3.2 Floating Point Unit (FPU)

The *Floating Point Unit* is an assist processor logically added to a system to improve the performance on floating-point operations. The processor can be on a separate chip (*e.g.*, PA-7000) or integrated onto the central CPU die (all PA-RISC CPUs upwards). The FPU executes special floating point instruction to perform arithmetic on its own set of independent registers (*register file*) and to move data between its own registers and the system's lower memory hierarchy. The FPU execution stage is pipelined. All PA-RISC FPUs contain thirty-two 64-bit registers, which can also be used as sixty-four 32-bit registers and sixteen 128-bit registers.

2.3.3 Transition Lookaside Buffer (TLB)

The *Translation Lookaside Buffer* is a hardware structure doing virtual-to-physical memory address translations. The TLB takes virtual page numbers and returns the corresponding physical page number. The PA-7000 is the last PA-RISC processor to use separate I/D TLBs, all later PA 1.1 and 2.0 CPUs use a combined TLB structure.

- ✧ PA-7000 - 96 I and 96 D entries
- ✧ PA-7100 - 120 combined entries
- ✧ PA-7100LC - 64 combined entries

⁴⁵ <http://burks.brighton.ac.uk/burks/pcinfo/hardware/cpu.htm>

- ◇ PA-7200 - 120 combined entries
- ◇ PA-7300LC - 96 combined entries
- ◇ PA-8000 - 96 combined entries
- ◇ PA-8200 (PCX-U+) - 120 combined entries
- ◇ PA-8500 (PCX-W) - 160 combined entries
- ◇ PA-8600 (PCX-W+) - 160 combined entries
- ◇ PA-8700 (PCX-W₂) - 240 combined entries
- ◇ PA-8800 - 2×240 combined entries
- ◇ PA-8900 - 2×240 combined entries

Hitachi's PA-RISC 1.1 derivatives also used split TLBs:

- ◇ Hitachi PA/50 - 32 I and 64 D entries
- ◇ Hitachi HARP-1 - 128 I and 128 D entries (some sources mention a second-level TLB)

Most interestingly, the older PA-RISC 1.0 processors (pre-PA-7000) have huge TLBs (even for today's standards):

- ◇ TS-1 - 4096 entries (split I/D)
- ◇ NS-1 - 4096 entries (split I/D)
- ◇ NS-2 - 16384 entries (split I/D)
- ◇ CMOS26B (PCX) - 8192 entries (split I/D)

The TLB memory on these earlier CPUs was implemented mostly off-chip/off-die via separate memory (SRAM) chips.

Translation process

- ◇ *PA 1.1*: If a virtual address has to be translated to a physical address, the corresponding TLB is searched for an entry matching the Virtual Page number. If an entry is found, the 20-bit Physical Page number, delivered by the TLB, is concatenated with the original 12-bit page offset to the build up the 32-bit absolute physical address.

TLB miss handling implementations

- ◇ *Hardware*: If the CPU implementation provides a hardware TLB miss handler, it attempts to find the virtual-to-physical translation in the *Page Table*. If successful, the translation and protection fields are inserted in the TLB. If not successful, an interruption occurs so the software miss handler can complete the translation.
- ◇ *Software*: If software TLB miss handling is implemented, a TLB miss fault interruption routine performs the translation. It inserts the translation and protection fields in the TLB and afterward restarts the interrupted routine, in which the TLB miss occurred.

2.3.4 Block Transition Lookaside Buffer (BTLB)

Similar as the TLB, the BTLB provides virtual-to-physical address translations. However the *BTLB* maps large address ranges rather than single pages as the *TLB* does. These large address ranges are called *block translations* and therefore stored in the *Block Translation Lookaside Buffer*. These block translations are useful for virtual address ranges that do not get paged in or out.

BTLBs were only implemented on 32-bit PA-RISC processors (PA-7x00), the 64-bit versions instead implement variable page sizes, thus any entry can be of >4k mapping.

2.3.5 Superscalar execution

Overview

A *superscalar* processor implementation decodes, dispatches and executes multiple instructions per cycle if dependencies between the instructions permit. This is possible if the instruction stream contains independent instructions. Superscalarity can be easily gained from an decoupled floating point unit (FPU) which executes floating point operations (calculations) independently from the (integer) ALU. More complicated variations allow for parallel load/store operations, integer calculations et al, which need a more complex CPU design that analyzes the instructions/branches.

Every PA-RISC processor from the PA-7100 upwards implements superscalar execution. Instructions proceed together through the execution pipeline which is called *instruction bundling*. The superscalar execution is functionally transparent to the software, the effects of any given instruction are the same whether it was executed as part of a *bundle* or alone. Bundling rules are applied at run-time by the hardware; optimal performance may only be gained by proper ordering of the instructions so the processor can use its full superscalar potential.

Several kinds of restrictions are placed upon the instruction bundling:

- ✧ Functional unit contention
- ✧ Data dependency restrictions
- ✧ Control flow restrictions
- ✧ Special instruction restrictions

For bundling purposes, all instructions are divided into classes:

Table 2.3: PA-RISC superscalar instruction classes

Class	Description
FLOP	Floating point operation
LDST	Loads and stores
ALU	Integer ALU
MM	Shifts, extracts, deposits
NUL	Might nullify successor
BV	Branch Vectored (BV) local, Branch (BE) external
BR	Other branches
FSYS	FTEST and FP status/exception
SYS	System control instructions

PA-7100 superscalar capabilities

The PA-7100 is two-way superscalar with one integer ALU and one FPU.

Allowed bundles

Table 2.4: PA-7100 allowed instruction bundles

First (older)instruction	Second (younger) instruction
ALU	+ FLOP
LDST	+ FLOP
FLOP	+ ALU/LDST/Branch

PA-7100LC/PA-7300LC superscalar capabilities

These are 2-way superscalar processor implementations with two integer ALUs and one FPU. Notably only one of the two ALUs is capable to handle loads, stores and shifts.

Allowed bundles

Table 2.5: PA-7100LC/PA-7300LC allowed instruction bundles

First (older)instruction	Second (younger) instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP
SYS	Never bundled

Besides from these bundles, *LDST + LDST* bundles are under certain circumstances also possible. These are then called *double word load/store*.

Data dependencies

Several kinds of instructions cannot be bundled together because of inter-instruction data dependencies:

- ✧ An instruction that modifies a register will not be bundled with another instruction that takes this register as operand.
Exception: a *FLOP* can be bundled with a FP store of the *FLOP*'s result register.
- ✧ A FP load to one word of a doubleword register will not be bundled with a *FLOP* that uses the other doubleword of this register.
- ✧ A *FLOP* will not be bundled with a FP load if both instructions have the same target register.
- ✧ An instruction that could set the carry/borrow bits will not be bundled with an instruction that uses carry/borrow bits.

Control Flow

- ✧ An instruction which is in the delay slot of a branch is never bundled with other instructions.

- ◇ An instruction which is at an odd word address and executed as a target of a taken branch is never bundled.
- ◇ An instruction which might nullify its successor is never bundled with this successor. Only if the successor is a *FLOP* instruction this bundle is allowed.

PA-7200 superscalar capabilities

This is a 2-way superscalar processor implementation. It has two integer ALUs and one FPU. Similar to the PA-7100LC, shift-merge and test condition units are not duplicated in the second ALU. To support the superscalar capabilities one additional write port and two additional read ports were added to the general registers (GR*).

Allowed bundles

Table 2.6: PA-7100LC/PA-7300LC allowed instruction bundles

First (older) instruction	second (younger) instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP

2.3.6 Multimedia Acceleration eXtensions (MAX-1 and MAX-2)

MAX-1 (32-bit)

The original multimedia extensions were proposed for and introduced in the PA-7100LC processor and later also available in the PA-7300LC. The aim was to enable workstations with this CPU to provide real-time MPEG video decompression and playback at a rate of 30 frames/second without the need for a special DSP (digital signal processing) chip.

The design process for the PA-7100LC processor (in the early mid-1990s) included for the first time multimedia benchmarks while analyzing optimizations for the instruction set design.

The actual implementation was achieved via the introduction of a very small set of SIMD-MIMD (*See Note 1*) instructions to facilitate the application of a small set of instructions on bundled subword data. Since these instructions use the same data paths and execution units within the processor as the “normal” instructions the term *intrinsic signal processing* (ISP) was coined. By sticking to conventional RISC principles the design team decided against adding complex special-purpose instructions and opted for small, elegant use of the existing processing facilities, which just were modified to understand the new, packed subword data.

In 1994, the extensions made their way to be included in the final PA-7100LC product and as such were the first SIMD (*See Note 1*) instructions found in a general microprocessor. Less than 0.2 percent of the silicon area had to be used for these additions and modifications, while allowing a very significant performance boost in affected applications (for example, the then-highend 735/99 workstation running at 99 MHz with 512KB cache achieves 18.7 fps at MPEG decompression benchmarks, while the new, lower clocked 712 workstation at 60MHz and with 64KB cache achieved 26 fps). New MAX-1 multimedia instructions include: parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average.

Notes

1. Single Instruction Multiple Data, Multiple Instruction Multiple Data (MIMD), see for example the [SIMD Wikipedia article](#)⁴⁶ and [MIMD Wikipedia article](#)⁴⁷

MAX-2 (64-bit)

With the introduction of the new 64-bit PA-RISC 2.0 architecture in 1996 HP unveiled a new set of multimedia-oriented instructions aimed at using the processor's resources more effectively for sub-word data. The basic components of the contemporary multimedia data were often represented as 8, 12 or 16-bit integers, for example audio sampling and pixel color depth. Doing arithmetic with data of this length would waste an considerable amount of the processor's execution capacities, a simple addition of 16-bit data would only use one quarter of the 64-bit wide integer units datapath. To remedy this situation, MAX allows for packing of these *subword data* into larger words near the processor's natural word width (64-bit on PA-RISC 2.0 processors) and using parallel instructions on them. An example would be four 16-bit additions by the 64-bit adder on four 16-bit packed subwords.

The basic functionality from the earlier 32-bit MAX-1 was taken over and four more instructions added for MAX-2. Additionally, due to the wider integer registers (now 64-bit) more subwords can be packed in one cycle, doubling the effective speed of these multimedia instructions. The MAX-2 multimedia instructions include (new in MAX-2 are in **bold**): parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average, **parallel shift right**, **parallel shift left**, mix and permute.

MAX-2 debuted 1996 with the PA-8000 processor and later featured on all subsequent PA-RISC 2.0 processors (PA-8x00). In contrast to contemporary multimedia extensions, MAX-2 required only very little die space (0.1 percent on the PA-8000).

References

- ✧ **Accelerating Multimedia with Enhanced Microprocessor**⁴⁸ (PDF, 2.4MB) Discussion of the MAX-1 instructions. Ruby Lee, April 1995, IEEE Micro, Volume 15 Number 2.
- ✧ **64-bit and Multimedia Extensions in the PA-RISC 2.0 Architecture**⁴⁹ (PDF, 66KB) New features of the 64-bit PA-RISC 2.0 architecture and overview on the MAX introduced with it. Ruby Lee and Jerry Huck, 1996, Hewlett-Packard Company.
- ✧ **Subword Parallelism with MAX-2**⁵⁰ (PDF, 1.5MB) Discussion of the MAX-2 instructions. Ruby Lee, August 1996, IEEE Micro, Volume 16 Number 4.

2.3.7 Further reading

Selected papers and articles for further reading on the PA-RISC architecture and platform

- ✧ **Hewlett-Packard Precision Architecture: The Processor**⁵¹ (.pdf) M. Mahon et al (August 1986: Hewlett Packard Journal. Accessed May 2009)

⁴⁶ <http://en.wikipedia.org/wiki/SIMD>

⁴⁷ <http://en.wikipedia.org/wiki/MIMD>

⁴⁸ <http://www.ee.princeton.edu/~rblee/HPpapers/accelMultimediawEnhancedMicroproc.pdf>

⁴⁹ <http://ftp.parisc-linux.org/docs/whitepapers/pa2c96.pdf>

⁵⁰ <http://homepages.cae.wisc.edu/~ece734/mmx/00526925.pdf>

⁵¹ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1986-08.pdf>

- ◇ **PA-RISC 1.1 Architecture and Instruction Set Reference Manual**⁵² (.pdf) Hewlett-Packard Company (February 1994, third edition. Accessed May 2009 at PA-RISC Linux FTP)
- ◇ **PA-RISC 2.0 Instruction Set Architecture**⁵³ (.pdf) Hewlett-Packard Company (1995. Accessed May 2009 at PA-RISC Linux FTP)

⁵² http://ftp.parisc-linux.org/docs/arch/pa11_acd.pdf

⁵³ <http://ftp.parisc-linux.org/docs/arch/parisc2.0.pdf>

2.4 PA-RISC Chipsets

2.4.1 Overview

Most HP PA-RISC computers use proprietary chipsets and system designs from HP. In the early 32-bit times workstations (the “HP 9000/700s”) and servers (“HP 9000/800s”) used different chipsets; later on, the system platforms of workstations and servers became more similar and used the same chipsets, albeit sometimes in different configurations.

The chipsets were tied to a specific bus architecture but were sometimes used in different generations of systems.

2.4.2 ASP

Used in

- ◇ 705, 710, 715, 725, 720, 730, 750
- ◇ 735, 755 (ASP2/Hardball)
- ◇ 742i, 745i, 747i

ASP is the chipset used in all older 32-bit PA-RISC workstations with the SGC bus. Still being a classical *chipset*, ASP includes several different chips to provide the I/O subsystem and several modules from third-party vendors.

There are two variants of ASP:

1. “Coral” or “Cobra I/O subsystem,” the original ASP
2. “Hardball” an improved ASP2 variant with fast/wide SCSI and FDDI networking, apparently used only on the 735/755 workstations

Features (ASP)

- ◇ VSC system main bus, 32-bit, to the Viper memory controller
- ◇ GSC main I/O bus (this is also sometimes called “SGC”)
- ◇ (Viper memory controller —sometimes counted into the ASP chipset and sometimes part of the CPU)
- ◇ NCR 53C700 8-bit Narrow single-ended SCSI-2
- ◇ Intel 82596DX 10Mb Ethernet controller
- ◇ Intel 82501AD Ethernet transceiver, media auto-selection
- ◇ Domain keyboard controller (not implemented on ASP2)
- ◇ WD 16C552 parallel
- ◇ NS 16550A compatible serial (three ports on ASP, two ports on ASP2)
- ◇ 512KB EPROM—the Boot ROM
- ◇ 8KB EEPROM for storing system configuration status etc.

- ◇ Intel 8042 microprocessor controlling:
 - Battery backed RTC
 - System & user timers
 - Audio generator
 - HP-HIL interface
 - Frontpanel system status LEDs
- ◇ 25-33MHz clock frequency
- ◇ 160-pin QFP chip (ASP)

ASP2 additional features

- ◇ NCR 53C720 16-bit Fast-Wide *differential* SCSI-2
- ◇ ASP2: AMD Formac Plus Am79C830 FDDI controller (ASP2)
- ◇ ASP2: Stereo/CD quality audio
- ◇ Two 32-bit device data buses (these are some variant of GSC bus)
 1. bus attaches to LAN an FDDI
 2. bus attaches to the two SCSI controllers, audio and via an 8-bit bus converter to the other I/O devices (serial, parallel, etc.)
- ◇ ASP2 consists of two separate chips (IOSS):
 1. **Shortstop** is the main data attachment to the VSC system main bus (and Viper memory controller) with 33MHz clock speed, produced in 0.8μ(micron) in CMOS (CMOS26B) packaged in 160-pin PLCC
 2. **Cutoff** is the main address controller with 33MHz clock speed, produced in 0.8μ(micron) in CMOS (CMOS26B) packaged in 240-pin PQFP

EISA bridges

Most systems with an ASP chipset feature a separate EISA bus, implemented with the Intel 82350 chipset (82352 EISA buffer, 82357 peripheral and 82358 controller). The EISA adapter is not integrated into or part of ASP but listed here since this configuration was only used with ASP systems.

References

1. **Midrange PA-RISC Workstations with Price/Performance Leadership**⁵⁴ (.pdf) Andrew J. DeBaets and Kathleen M. Wheeler (August 1992: Hewlett-Packard Journal) pp. 6-11
2. **VLSI Circuits for Low-End and Midrange PA-RISC Computers**⁵⁵ (.pdf) Craig A. Gleason (August 1992: Hewlett-Packard Journal) pp. 12-22

⁵⁴ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

⁵⁵ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

3. **High-Performance Design for Low-Cost PA-RISC Desktops**⁵⁶ (.pdf) Craig Fink et al (August 1992: Hewlett-Packard Journal) pp. 56-63
4. **Hardball I/O Subsystem, External Reference Specification**⁵⁷ (.pdf) Hewlett-Packard Company (September 1991, Version 1.1)
5. **The EISA standard for the HP 9000 Series 700 workstations**⁵⁸ (.pdf) Vicente Cavanna and Christopher S. Liu (December 1992, Hewlett-Packard Journal) pp. 78

2.4.3 LASI

Used in

- ◇ 712, 715, 725
- ◇ 743i, 745, 744, 748i
- ◇ A180, A180C
- ◇ B132L, B132L+, B160L, B180L+
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- ◇ D-Class
- ◇ E25, E35, E45, E55
- ◇ J200, J210, J210XC, J280, J282, J2240
- ◇ K-Class
- ◇ RDI PrecisionBook 132, 160, 180
- ◇ R380, R390
- ◇ SAIC Galaxy 1100

Designed for and first used in the HP 9000/712 workstations the LASI I/O controller was designed for cost-reductions. The major objective of the 712 I/O subsystem was to provide similar or equal functionality and performance as other 700 series systems (*e.g.*, 720, 730, 715) at reduced production costs. The integration of major I/O subsystems into one large chip would reduce manufacturing costs significantly. Large parts of the LASI chip are consumed by the logic of the important LAN and SCSI (LASI: LAN SCSI) parts. Both of these designs are third party (NCR and Intel). The other I/O functions are HP-internal standard cell designs, some of whom were taken from previous HP ASIC designs and some designed specifically for LASI. In early systems LASI was used as main I/O controller, in later systems it acted as complimentary part for some of the I/O functions.

Features

- ◇ LAN controller — Intel i82C596CA 10Mb Ethernet controller
- ◇ SCSI controller — NCR 53C710 Fast-Narrow SE SCSI-2 controller
- ◇ Serial interface — NS16550A compatible RS232

⁵⁶ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

⁵⁷ http://ftp.parisc-linux.org/docs/chips/hardball_ers.pdf

⁵⁸ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-12.pdf>

- ◇ Parallel—WD16C522 compatible
- ◇ Audio—*Harmony* CD-quality 16-bit sound
- ◇ Telephony—optional expansion, support for two lines
- ◇ Human Interface—support for two PS/2 style keyboard and mouse devices
- ◇ FDD and boot ROM—external 8-bit bus to connect flash EPROMs and a FDD controller (WD37C65C)
- ◇ Interface to GSC bus
- ◇ Bus arbitration
- ◇ Interrupt controller
- ◇ Real-Time clock (RTC)
- ◇ PLL generator for the whole I/O subsystem
- ◇ Up to four LASI chips can be used on a single GSC bus (however apparently never implemented)
- ◇ Supports both 3.3V and 5.0V PCI operation
- ◇ 13.2×12.0 mm² die, 520,000 FETs, 0.8μ(micron), CMOS (HP CMOS26B process), packaged in 240-pin MQUAD
- ◇ 3W power consumption at 40MHz

References

1. 712 I/O Subsystem ERS (External Reference Specification)—“LASI ERS”⁵⁹ Hewlett-Packard Company (February 1993, Revision 1.1)
2. An I/O System on a Chip⁶⁰ Thomas V. Spencer et al (April 1995, Hewlett-Packard Journal)

2.4.4 Wax

Used in

- ◇ 715, 725
- ◇ 743i, 745, 744, 748i
- ◇ B132L, B132L+, B160L, B180L+
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- ◇ D-Class
- ◇ E25, E35, E45, E55
- ◇ J200, J210, J210XC, J280, J282, J2240
- ◇ R380, R390

⁵⁹ http://ftp.parisc-linux.org/docs/chips/lasi_ers.pdf

⁶⁰ <http://www.hpl.hp.com/hpjournal/95apr/apr95a4.pdf>

Wax is a secondary I/O controller complimentary to the LASI chipset. It implements various secondary I/O functions and acts as a I/O bus to GSC adapter for different external buses as EISA, HP-HIL and HP-IB. Most systems use it to complement LASI with other needed I/O functions that were previously implented in diverse I/O ASICs. It is implemented in the same process and package as LASI.

Features

- ◇ GSC bus interface with GSC+ features
- ◇ EISA bus converter
 - Interfaces GSC to the 32-bit EISA, so EISA devices can attach
 - Does not provide complete EISA bus conversion—provides an “Intel i486-like” bus interface, to which external EISA chips attach
 - Interfaces to external EISA controller: TI TACT84500 (provides EISA bus control unit EBCU and EISA peripheral control unit EPCU)
 - Integrates the EDPU (EISA data path unit) functionality on-chip
 - Attaches to i486 bus for control, bus and IRQ, and directly to EISA for data
 - Can be switched at power up to operate as ISA controller (to directly interface with ISA-only devices such as Token Ring controllers etc.)
- ◇ Serial interface—NS16550A compatible RS232 (software-compatible with LASI circuitry)
- ◇ HP-HIL interface, compatible to previously separate HP HIL chip (1820-4784) used in older workstations
- ◇ HPIB interface for instrumentation devices, needs three external chips
- ◇ Interrupt control
- ◇ Timers (real time, watchdog)
- ◇ 0.8μ(micron) CMOS (HP CMOS26B process), packaged in 240-pin MQUAD
- ◇ Wax chip numbers: 1FT4-0001

References

1. **External Reference Specification (ERS) for the Wax I/O ASIC**⁶¹ Hewlett-Packard Company (May 1993, version 1.0 redacted)

2.4.5 Dino/Cujo

Used in

- ◇ A180, A180C
- ◇ B132L, B132L+, B160L, B180L+
- ◇ C132L, C160L, C160, C180, C200, C240, C360

⁶¹ http://ftp.parisc-linux.org/docs/chips/WAX_ERS_V1.0_Redacted.pdf

- ◇ J2240
- ◇ RDI PrecisionBook 132, 160, 180

Dino is the GSC to PCI bridge found in many older PCI PA-RISC workstations. The GSC and PCI buses do not need to be synchronized, simplifying the system design. Dino also implements a small set of I/O functions.

Cujo is a Dino bridge with 64-bit PCI.

Features

- ◇ GSC bus interface with GSC+ features
- ◇ Mapping register with 8MB resolution
- ◇ Integrated PCI arbitration
- ◇ Integrated interrupt register
- ◇ Supports >40MHz GSC operation
- ◇ Supports >33MHz PCI operation
- ◇ Two PS/2 interfaces
- ◇ RS-232 port
- ◇ Supports both 3.3V and 5.0V PCI operation
- ◇ 208-pin PQFP package
- ◇ Dino chip numbers: 1FC3-0004

References

1. DINO ERS (External Reference Specification) — A GSC-to-PCI Bridge⁶² Hewlett-Packard Company (February 1997, Revision 3.0)
2. Dino 3.1 (1FC3-0004) Errata Listing⁶³ Hewlett-Packard Company (September 1997)

2.4.6 Elroy

Used in

- ◇ A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- ◇ B1000, B2000, B2600
- ◇ C3000, C3600, C3700
- ◇ J5000, J5600, J6000, J6700, J7000, J7600
- ◇ L1000 (rp5400), L2000 (rp5450)

⁶² http://ftp.parisc-linux.org/docs/chips/dino_ers.pdf

⁶³ http://ftp.parisc-linux.org/docs/chips/Dino_3_1_Errata.html

- ◇ L1500 (rp5430), L3000 (rp5470)
- ◇ N4000 (rp7400)
- ◇ N4000 (rp7405, rp7410)
- ◇ rp3410, rp3440
- ◇ rp4410, rp4440
- ◇ rp7420
- ◇ Superdome

Elroy is the chip used to attach a PCI bus to the system and I/O buses in the various newer PA-RISC systems. Each Elroy chip attaches one PCI bus to one or more of the I/O system's I/O channels — ropes. Common configurations are one I/O link (about 250MB/s) for one “Turbo” PCI bus (can have multiple slots or attach multiple I/O devices) or two I/O links (about 500MB/s) for one *Twin Turbo* bus.

Elroy is also called LBA one some of the newer systems.

Features

- ◇ Peak bandwidth of up to 500MB/s
- ◇ Attaches to one or more I/O links — ropes
- ◇ Provides one PCI bus
- ◇ Multiple Elroys can be used in a single system
- ◇ Support for *Turbo* and *Twin Turbo* slots — attached via one or two links respectively
- ◇ Support for PCI 2.1, 1X, 2X and 4X protocol
- ◇ PCI data width of 32 or 64 bit
- ◇ PCI clock of 33 or 66MHz

References

1. Elroy ERS (External Reference Specification)—Ropes to PCI Bridge Chip⁶⁴ Hewlett-Packard Company (January 2000, Revision A (1.4))

2.4.7 SIU/SPI

The first PA-RISC processors (PA-RISC 1.0) did not have integrated, unified memory and I/O controllers but used several external support chips to attach the CPU to and control the memory and I/O.

The bus setup and structure was similar on all three NS-1, NS-2 and PCX processors and utilized the SMB CPU attachment but several variants of supports chips.

NS-1:

- ◇ SIU (system interface unit) attaches the CPU to the SMB system main bus (64-bit)

⁶⁴ http://ftp.parisc-linux.org/docs/chips/elroy_ers.pdf

- ◇ Two CCUs (cache controller units CCU₀ and CCU₁) for the cache access
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ Memory is attached to the SMB main bus
- ◇ I/O is attached to the SMB main bus (with two 32-bit converters over the CTB)
- ◇ Cache is attached to the CCUs which attach to the CPU

NS-2:

- ◇ SIU (system interface unit) for the system and memory bus
- ◇ Two CCUs (cache controller units, split into instruction and data—ICCU and DCCU)
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ Memory is attached to the SMB main bus
- ◇ I/O is attached to the SMB main bus (with two 32-bit converters over the CTB)
- ◇ Cache is attached to the CCUs which attach to the CPU

PCX:

- ◇ SPI (SMB to processor interface)
- ◇ Three CMUX (cache multiplexer—one instruction, two data)
- ◇ Physical address space of 29-bit (512MB main memory could be addressed)
- ◇ Memory is attached to the SMB main bus
- ◇ I/O is attached to the SMB main bus (with two 32-bit converters over the CTB)
- ◇ Cache is attached to the CMUXs which attach to the CPU

2.4.8 Viper

Viper is the external single external memory and I/O controller (MIOC) on systems with PA-7000 and PA-7100 processors. The chip is apparently similar on both, and sometimes counted into the ASP I/O chipset.

Viper interfaces with PBus to the processor and VSC to the system main bus. It handles all memory and I/O traffic between the processor and the rest of the system.

Bus attachments

- ◇ Viper attaches with 32-bit multiplexed address/data bus (PBus) to the CPU
- ◇ Memory attaches directly to Viper, with multiplexed 64-bit ECC
- ◇ VSC system main bus attaches to Viper (32-bit on PA-7000, 64-bit on PA-7100)
- ◇ System main bus interface via two custom ASICs (system bus interface SBI)
- ◇ I/O attaches with bus adapters to VSC bus

Details

- ✧ Also called **Memory and I/O controller (MIOC)**, **Processor Memory Interface (PMI)** and **Processor Interface Chip (PIC)**
- ✧ On SMP systems two connections strategies supported: Each CPU has its own MIOC which share a SMB bus and memory, or two CPUs share one MIOC
- ✧ 9,5×9,5 mm² die, 185,000 FETs, 0.8μ(micron), CMOS (CMOS26B) in 272-pin CPGA
- ✧ SBI: two 100-pin QFP chips
- ✧ Viper was implemented in a low-cost version on the 705/710 workstations: two separate chips, each 7,0×7,0 mm² die, 1.0μ(micron), two-layer metal CMOS (CMOS34) in 160-pin QFP
- ✧ Viper (PA-7000) chip numbers: 1FV8-0002

References

1. **Midrange PA-RISC Workstations with Price/Performance Leadership**⁶⁵ (.pdf) pp. 6-11 Andrew J. DeBaets and Kathleen M. Wheeler (August 1992: Hewlett-Packard Journal)
2. **VLSI Circuits for Low-End and Midrange PA-RISC Computers**⁶⁶ (.pdf) pp. 12-22 Craig A. Gleason (August 1992: Hewlett-Packard Journal)
3. **High-Performance Design for Low-Cost PA-RISC Desktops**⁶⁷ (.pdf) pp. 56-63 Craig Fink et al (August 1992: Hewlett-Packard Journal)

2.4.9 Memory and I/O Controller (MIOC)

The *Memory and I/O Controller* in the PA-7100LC processor and PA-7300LC processor is the integration of both DRAM/cache controller and I/O controller on the processor die. It is very similar on both CPUs, not much has been changed in the transition from 7100LC to 7300LC.

The integrated memory controller requires only buffers and DRAM modules to build up the complete memory subsystem.

- ✧ Execution units and internal caches attach on-chip to the MIOC
- ✧ External cache (L1 on PA-7100LC, L2 on PA-7300LC) attach to MIOC via 64-bit (PA-7100LC) or 128-bit (PA-7300LC), both with ECC
- ✧ Memory attaches to MIOC via 64-bit (on PA-7100LC) or 128-bit (PA-7300LC), with ECC
- ✧ On PA-7300LC memory lines use the L2 cache data lines
- ✧ GSC, the system main bus attaches to MIOC
- ✧ On PA-7300, GSC+ system main bus
- ✧ Support for 4, 16, 64 and 256 Mbit modules
- ✧ Support for both FPM and EDO DRAM

⁶⁵ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

⁶⁶ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

⁶⁷ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

- ◇ Optional SEDC error control
- ◇ Up to 16 physical memory slots
- ◇ Support for a wide range of core frequencies
- ◇ Support for 3.3V and 5.0V DRAM

On the PA-7300LC the memory controller also includes the SLC (*Second Level Cache Controller*). It provides an *optional* L2 cache, ranging from 32KB to 8MB (on almost all systems with a PA-7300LC, 2MB of L2 was used). It shares the data bus with the DRAM subsystem, so it has the same width (64/128-bit) and same optional SEDC error control.

2.4.10 U2/Uturn

The U2/Uturn I/O adapters (IOAs) attach the I/O adapters and buses (GSC) to the Runway CPU bus on systems with the PA-7200, PA-8000 and PA-8200 processors.

On the I/O side they provide two GSC (HSC) buses to which other I/O chips and bridges or chipsets attach. Systems with PA-7200 use the U2 variant while all later systems the UTurn follow-on.

Details

- ◇ A single UTurn/U2 consists of two separate integrated I/O adapters bridges — IOA A and IOA B
- ◇ Runway bus interface to CPU/memory bus, 64-bit wide, 120MHz, 960MB/s peak bandwidth
- ◇ Two GSC/HSC buses to I/O, each raw I/O bandwidth between 128MB/s to 160MB/s
- ◇ Support for various frequencies on both sides (Runway and GSC)
- ◇ Address translation from 32-bit GSC to 40-bit Runway addresses
- ◇ Hardware cache coherent I/O
- ◇ Interface to processor dependent hardware (PDH) — on IOA A
- ◇ Real-time clock
- ◇ U2 is a 432-pin PGA chip
- ◇ U2 chip numbers: 1MM6-0004

References

- ◇ **Visualize J200, J210 technical reference manual**⁶⁸ (.pdf) p. 23 (2-2) Hewlett-Packard (September 1996)
- ◇ **Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost**⁶⁹ (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)

⁶⁸ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37962/lpv37962.pdf>

⁶⁹ <http://www.hpl.hp.com/hpjournal/96feb/feb96a1.pdf>

2.4.11 MMC/SMC

Most systems with a PA-7200, PA-8000 or PA-8200 processor use a combination of the MMC and SMC memory controllers to attach the main system memory to the Runway processor bus. The I/O is controlled by the U2/UTurn I/O adapters on the same Runway bus.

Details

- ✧ **Master Memory Controller (MMC)** is the main memory controller and attaches with 64-bit to the Runway processor bus and 128-bit to the memory data bus (via the DMs)
- ✧ **Slave Memory Controllers (SMCs)** are the secondary memory controllers and attach to the MMC main memory controllers. Up to eight SMCs attach to one MMC on its memory address bus. The SMCs carry the functionality to interface with specific types of DRAM.
- ✧ **Data Multiplexers (DMs)** attach the 128-bit 60MHz data bus of the MMC to the four sets of memory. Each two sets of memory connect with two 64-bit 30MHz buses to the DMs. The DMs are not used in all systems.
- ✧ Memory data bus from MMC to DMs/memory 128-bit wide, with 60MHz peak bandwidth (960MB/s data rate)
- ✧ Physical address space of 36-bit (32GB main memory)
- ✧ Memory address bus is shared between all SMCs of a MMC, 39-bit at 60MHz
- ✧ Memory data bus attaches to the DMs and memory
- ✧ Memory attaches to their private SMCs for addresses and to Data MUXes for data
- ✧ Up to 32-way memory interleaving (four-way per SMC)
- ✧ MMC is a 432-pin PGA chip
- ✧ SMCs are 208-pin MQUAD chips
- ✧ DMs are 160-pin POFP chips

Used in

- ✧ C100, C110, C160, C180, C200, C240, C360
- ✧ D-Class
- ✧ J200, J210, J210XC, J280, J282, J2240
- ✧ K-Class

References

- ✧ **A New Memory System Design for Commercial and Technical Computing Products**⁷⁰ (.pdf)
Thomas R. Hotchkiss, Norman D. Marschke, and Richard M. McClosky (Februar 1996: Hewlett-Packard Journal)
- ✧ And cf. the references of U2/UTurn above

⁷⁰ <http://www.hpl.hp.com/hpjjournal/96feb/feb96a5.pdf>

2.4.12 Astro

Used in

- ◇ A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- ◇ B1000, B2000, B2600
- ◇ C3000, C3600, C3700
- ◇ J5000, J5600, J6000, J6700, J7000, J7600
- ◇ L1000 (rp5400), L2000 (rp5450)

Newer workstations and servers, based on the PA-8500, PA8600 and 8700 processors, use the Astro chip for memory and I/O management (IOMMU). It includes most of the functions on a single die with only few additional peripheral ASICs to interface and drive the specific buses.

Astro attaches to three different buses and is the central part of the chipset:

References

1. Processor system bus—Runway+/Runway DDR for (theoretically) up to two (apparently four were possible) PA-8x00 processors with a clock of maximum of 125MHz (and peak bandwidth of about 2.0GB/s)
2. Memory bus with a peak bandwidth of 2.0GB/s at maximum clock of 125MHz
3. I/O system buses made up from up to eight single I/O links (*ropes*) which attach to individual PCI bridges—in most cases Elroy chips which convert each one or two I/O links into a PCI bus

There are several different variants of Astro, later ones were called **Pluto**.

Features

- ◇ System/processor bus bandwidth of peak 2.0GB/s, sustainable 1.5GB/s, via 64-bit Runway+/Runway DDR bus at maximum of 125MHz in DDR mode
- ◇ Memory bandwidth of peak 2.0GB/s, sustainable 1.5GB/s (a variant of Runway)
- ◇ Up to two or four processors [two were stated in the documentation but four actually implemented in the L2000 server—*Ed.*]
- ◇ Up to eight I/O links (*ropes*)—each 10-bit, 133MHz with datarate of 250MB/s; aggregate maximum 2.0GB/s
- ◇ Support for 120/125MHz SDRAMs
- ◇ Maximum supported memory of 40GB
- ◇ PCI 2.1 compliant
- ◇ 16-entry fully associative I/O TLB
- ◇ 16-entry fully associative coherent I/O buffer cache
- ◇ 664-pin ceramic LGA

- ◇ Generates about 20W
- ◇ Astro chip numbers: 1QM2-0004, 1ST8-0002

References

1. **Astro External Reference Specification Introduction**⁷¹
Astro External Reference Specification Error Handling⁷²
Astro External Reference Specification R2I Operations⁷³
Astro External Reference Specification Register Map⁷⁴
Astro External Reference Specification Runway Interface⁷⁵
Astro External Reference Specification Memory Map⁷⁶
 Hewlett-Packard Company (February 2000, Revision 1.2)

2.4.13 Stretch

Used in

- ◇ L1500 (rp5430), L3000 (rp5470)
- ◇ N4000 (rp7400)

Stretch is the chipset or “Central Electronics Complex” (CEC) used in a very small range of systems. It basically consists of four main components, which build the backbone of the (Runway-based PA-8x00) processor/memory and I/O system—one central memory controller which connects all system buses together; Runway ports for attachment of processors to the system bus; I/O controllers which attach the I/O subsystem to the system bus; PCI bridges, which convert the I/O subsystem’s links into PCI buses:

1. **Prelude SMC memory controller** is the central part of the system, it connects the main memory to two system buses (one on each side), to which each one IKE I/O controller and one or more DEW Runway ports (for each two CPUs) attach (Prelude is also called “Very Low Latency Memory Controller”)
2. **DEW Runway ports/converters** convert the Prelude’s system bus(es) (which in fact is an Itanium/Merced bus) into Runway buses for the various CPUs—each two CPUs share one DEW port converter (CPUs from the PA-8500 upwards supported). Common configurations include 1-4 DEWs for up to eight processors.
3. **IKE I/O controllers** attach each to the system bus. Common configurations are one IKE for each of the two system buses (one on each side). IKEs then connect to the various PCI bridges.
4. **Elroy PCI bridges** (LBAs) which convert the I/O channels from the IKE I/O controllers into PCI buses, to which the PCI slots and core I/O functions attach. Up to 14 Elroys were used in actual systems.

⁷¹ http://ftp.parisc-linux.org/docs/chips/astro_intro.pdf

⁷² http://ftp.parisc-linux.org/docs/chips/astro_errors.pdf

⁷³ http://ftp.parisc-linux.org/docs/chips/astro_ioc.pdf

⁷⁴ http://ftp.parisc-linux.org/docs/chips/astro_regmap.pdf

⁷⁵ http://ftp.parisc-linux.org/docs/chips/astro_runway.pdf

⁷⁶ http://ftp.parisc-linux.org/docs/chips/astro_sysmap.pdf

Features

- ◇ Two system buses 133MHz, each 2.1GB/s peak — aggregate 4.3GB/s (these system buses are Itanium/Merced system buses)
- ◇ Up to four memory buses, each 2.1GB/s peak — aggregate 8.6GB/s bandwidth to the memory (on the rp7400)
- ◇ DEW port converters for attachment of PA-8x00 processors with Runway to the Merced system bus — up to four DEWs were found in actual systems
- ◇ I/O controllers attach to the system bus
- ◇ Multiple I/O channel configurations from the IKE I/O controller(s) supported — each 133MHz 256MB/s with eight, twelve or 22 links found in actual systems (2.1GB/s, 3.2GB/s or 6.4GB/s aggregate max bandwidth)

References

- ◇ *hp server rp7400 whitepaper*, Hewlett-Packard Company (February 2002, product number 5981-0154EN) [did not find an appropriate URL for this PDF document — *Ed.*]
- ◇ **rp7400 Hardware Manual**⁷⁷ (PDF) Hewlett-Packard Company (May 2002)
- ◇ *hp server rp5400 series entry-level UNIX servers technical whitepaper*, Hewlett-Packard Company (August 2002) [did not find an appropriate URL for this PDF document — *Ed.*]

2.4.14 Cell

Used in

- ◇ N4000 (rp7405, rp7410)
- ◇ Superdome

The Superdome and various smaller systems from HP used a *cell-based* system architecture or “Central Electronics Complex” (CEC) which was based on interconnecting individual system/processor cells via central crossbars. The cell boards were seated in the backplane of the system, which provided the cell-to-cell links and I/O functionality.

1. **Cell controller (CC):** the central chipset and crossbar of these systems. One sits at the centre of each cell board for a maximum of two in the complete system. The CCs provide links for:
 - ◇ Up to four Processors (8.0GB/s)
 - ◇ Up to two Memory “banks” (4.0GB/s peak)
 - ◇ I/O via SBA (cell to I/O communication is 2.0GB/s peak)
 - ◇ PDH (processor dependent hardware) and firmware/flash etc.
 - ◇ Second cell via XBC (cell-to-cell communication is 8.0GB/s peak)

⁷⁷ http://docs.hp.com/en/3687/rp7400_customer_hardwaremanual.pdf

2. **Master I/O controller (SBA):** the central I/O part of the main chipset, normally one SBA is reserved for each one cell/CC but located on the (I/O) backplane. Each SBA provides sixteen 12-bit links (“ropes”) — the links/ropes from the SBAs connect to slave I/O controllers (**LBAs**) which in turn connect the PCI I/O slots and I/O subsystems
3. **Core I/O:** provides the standard I/O functions for the system. Made up of cards or card sets, which plug into PCI or special slots and provide third-party I/O functions. Distinct cards were available/possible: MP/SCSI card and LAN/SCSI, among others. These cards contain a variety of I/O chips, including Ultra160 SCSI, Ultra2-Wide SCSI, Gigabit Ethernet LAN. Ethernet for management LAN, serial ports for management and console, etc.

Other parts of the chipset are made up from already known components:

- ◇ Prelude SMC memory controllers (on each cell board) from the Stretch chipset (used in earlier N4000s and L1500/L3000)
- ◇ Elroy PCI bridges (**LBAs**) convert the links/ropes from the SBA into PCI bus

References

- ◇ *hp server rp7410 whitepaper*, Hewlett-Packard Company (March 2002, product number 5980-9997EN) [did not find an appropriate URL for this PDF document — *Ed.*]
- ◇ **User Guide hp rp7405/7410 Servers**⁷⁸ (PDF) Hewlett-Packard Company (2002, third edition)

⁷⁸ <http://docs.hp.com/en/A6752-96008/A6752-96008.pdf>

2.5 PA-RISC Buses

2.5.1 EISA

The *Extended ISA* bus replaced ISA in HP Unix systems. EISA buses are available in several older 32-bit workstations, either on-board or through a converter, which made it possible to use third-party, generic expansion cards.

- ◇ 32-bit data path width
- ◇ 33MB/s maximum data rate
- ◇ 5V signalling voltage
- ◇ EISA slots also accept 8/16-bit ISA cards
- ◇ 200-pin(50×2×2) edge male card connector
- ◇ Bulkhead is left of the card

2.5.2 SGC

The *System Graphics Connect* is the main system bus of the older 32-bit series 700 workstations. Thus SGC expansion cards directly attach to the main bus in these systems. Cards were manufactured in two different form factors/sizes: *EISA* and *DIO*.

- ◇ 32-bit data path width
- ◇ 100MB/s maximum data rate
- ◇ 5V signalling voltage
- ◇ 176-pin (44×4) female pin&socket card connector (*DIO-II FF*)
- ◇ 160-pin (40×4) male EDDL card connector (*EISA FF*)
- ◇ Bulkhead is above the card (*DIO-II FF*)
- ◇ Bulkhead is right of the card (*EISA FF*)

References

1. **HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC**⁷⁹ (p. 195) Hewlett-Packard Company (July 1998, 14th ed.)

2.5.3 HP-PB

The *HP-Precision Bus* is the I/O bus in many older 32-bit series 800 servers. There are two form factors/sizes of HP-PB expansion cards: *single* and *double*.

- ◇ 32-bit data path width
- ◇ 23MB/s maximum data rate

⁷⁹ <http://ftp.parisc-linux.org/docs/platforms/980723.pdf>

- ◇ 5V signalling voltage
- ◇ 96-pin (32×3) female pin+socket card connector

References

1. **HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC⁸⁰** (p. 190) Hewlett-Packard Company (July 1998, 14th ed.)

2.5.4 PCI

With the PCI bus HP changed the HP 9000 design to use an industry standard expansion and device bus. This made it possible to use cheaper COTS products such as I/O chips and cards without having to build (HP-proprietary) GSC/SGC interfaces. Some of HP's PCI expansion cards for HP 9000 computers are relabeled third-party products or OEM designs with a PA-RISC compatible firmware and HP-UX driver.

Proper HP-UX drivers are the limiting factor for generic third-party PCI expansion cards in PA-RISC systems. In most cases HP supplied drivers only for their own HP-branded products. This prevents using common storage or networking adapters from the PC world, since no proper HP-UX drivers are available.

Open source operating systems as Linux or OpenBSD support much more varied expansion cards on their PA-RISC ports, since many drivers could be ported or taken over from other architectures.

Table 2.7: PCI buses used in PA-RISC computers overview

PCI	Clock	Width	Data ratemax	Signalling
PCI-32/33	33MHz	32-bit	133MB/s	3.3V/5V
PCI-32/66	66MHz	32-bit	266MB/s	3.3V
PCI-64/33	33MHz	64-bit	266MB/s	3.3V/5V
PCI-64/66	66MHz	64-bit	533MB/s	3.3V
PCI-X	66MHz	64-bit	533MB/s	?
PCI-X	100MHz	64-bit	800MB/s	3.3V
PCI-X	133MHz	64-bit	1066MB/s	?

Any PCI card should run in any PCI slot if the voltage (3.3V or 5V) is correct. Slower cards in faster slots will reduce the overall PCI bandwidth of that particular bus.

2.5.5 GSC/HSC

The *General System Connect* bus is the primary system and I/O bus on most of the older, “numbered” HP 9000/700 workstations. It connects most of the I/O devices to the system bus and central chipset. Some CPUs directly attach to GSC (PA-7100LC and PA-7300LC; see below). HSC is a variant of GSC but electronically the same bus.

GSC bus features

- ◇ 32-bit data path width

⁸⁰ <http://ftp.parisc-linux.org/docs/platforms/980723.pdf>

- ◇ Multiplexed address and data
- ◇ Transfer rates of up to 142-256MB/s (depending on bus variant — see below)
- ◇ 5V signalling voltage

Bus variants

1. Original GSC (GSC-1X) with peak data rate 142MB/s
2. GSC+ (“Extended GSC”) with a maximum clock of 40MHz and peak data rates of 160MB/s (132MB/s with 33MHz, 144MB/s with 36MHz)
3. GSC-1.5X with additional extended write operations
4. GSC-2X with a peak data rate of 256MB/s

Expansion cards variants

- ◇ EISA-like
 - Both GSC-1X and GSC-2X (also probably GSC-1.5X)
 - 100-pin (50×2) female EDDL card connector
 - Bulkhead is left of the card
- ◇ GIO
 - Limited to the 712 workstation
 - GSC-1X
 - 80-pin (40×2) female EDDL card connector (*GIO FF*)
 - Bulkhead is right of the card (*GIO FF*)
- ◇ HSC (“High-speed System Connect”)
 - On several server systems, for example D-Class and K-Class
 - Cards are all GSC+
 - 100-pin (50×2) male pin & socket with groundplane
 - Bulkhead is above the card
 - Identical to GSC-M cards except different bulkhead (external connections plate)
- ◇ GSC-M (“Mezzanine”)
 - Found on PA-RISC VME computers (74x)
 - GSC-1X
 - 100-pin (50×2) male pin & socket with groundplane
 - Bulkhead is below the card
 - Cards are very rare
 - Identical to HSC cards except different bulkhead (external connections plate)

CPU attachments

The two 32-bit LC “Low Cost” processors PA-7100LC and PA-7300LC integrate the previously external memory and I/O controller (MIOC) on the processor itself. This allowed for the processor to directly attach to the main system bus, in this case the GSC bus (which mostly was used with LASI chipsets). Memory and cache directly attach to the processor with its integrated MIOC. Both PA-7100LC and PA-7300LC were not multi-processor capable.

1. MIOC is the main memory and I/O controller directly integrated on the CPU
 - ✧ Execution units and internal caches attach on-chip to the MIOC
 - ✧ External cache and memory attach to MIOC
2. GSC, the system main bus, attaches to MIOC and various I/O controllers
 - ✧ Attaches via 32-bit
 - ✧ PA-7300LC systems use the extended GSC+
3. I/O adapters attach to GSC
 - ✧ LASI chipset
 - ✧ Some video adapters directly attach to GSC
 - ✧ I/O slots extend GSC
 - ✧ Bus adapters, including EISA, VME and PCI, attach to GSC (includes WAX—a modified LASI—, Dino, and custom chips)

References

1. PA-RISC Linux: Glossary⁸¹ The PARISC-Linux Project (May 2005)
2. HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC⁸² (pp. 188-189, 191, 198)
3. Hewlett-Packard Company (July 1998, 14th ed.)

2.5.6 VSC

The *Viper System Connect* bus is the central system bus of computers with the PA-7000 or PA-7100 processors. It connects the Viper central bus controller (known as MIOC, PMI or PIC, interfaces to the main processor) to the memory and I/O buses (via adapters). In multiprocessor configurations, each processor has its own Viper controller, which then in turn connect to a *shared* VSC bus, which has attachments to all Viper controllers, the memory and the I/O converters. It is also known as PMB—Processor Memory Bus—especially on multi-processor configurations.

- ✧ 32-bit data path width on PA-7000 systems
- ✧ 64-bit data path width on PA-7100 systems
- ✧ 128-bit data path was theoretically possible but apparently never implemented
- ✧ Synchronous pipelined bus

⁸¹ <http://parisc-linux.org/hardware/supported.html>

⁸² <http://ftp.parisc-linux.org/docs/platforms/980723.pdf>

- ◇ Separate data and address buses
- ◇ Memory data blocks are transferred in 16, 32 or 64 Byte blocks
- ◇ Provides cache and TLB coherency on multi-processor configurations as a snoopy bus
- ◇ Various clock speeds were supported, as a ratio of the processor clock speed (2/3 was common [or maybe the maximum — *Ed.*])
- ◇ Maximum data rate depends on clock speed and bus width, with common 60MHz and 64-bit: 480MB/s
- ◇ Apparently 3.0V signalling voltage

References

1. **Corporate Business Servers: An Alternative to Mainframes for Business Computing**⁸³ (.pdf)
Thomas B. Alexander et al (June 1994: Hewlett-Packard Journal)

2.5.7 System Main Bus (SMB)

In early PA-RISC (1.0) systems with the NS-1, NS-2 and PCX processors the CPU attaches via bus converters to the System Main Bus.

Bus features

- ◇ 64-bit data width
- ◇ Clockspeed of maximum 25-30MHz
- ◇ Central system bus between CPU/bus adapter, memory and I/O buses

CPU attachment

1. **System controllers (SIU or SPI)** attach the CPU with its execution units to the SMB system main bus
2. **System Main Bus (SMB)** is the central bus, to which CPU, memory and I/O buses attach
 - ◇ CPU attaches via SIU/SPU to SMB with 64-bit at 25-30MHz
 - ◇ Memory attaches to SMB
 - ◇ (Some) Memory extensions attach to SMB (via MABs; see below)
3. **Central Bus/Midbus (CTB)** attaches the I/O via bus convertes to SMB
 - ◇ Attaches via 32-bit at maximum of 10MHz at SMB
 - ◇ Two CTBs per SMB
4. **CIO buses** (up to three) attach via adapters to CTB
 - ◇ Attaches via 16-bit at 4MHz (probably dependant on CTB clock)

⁸³ <http://www.hpl.hp.com/hpjjournal/94jun/jun94a1.pdf>

- ◇ I/O expansion cards plug into CIO slots

5. (Some systems only) **Memory Array Buses** (MABs) attach to SMB for more memory

- ◇ Attaches via 72-bit (ECC) at SMB

The TS-1, the first PA-RISC processor used a simpler version of this setup and directly attached the CPU to the Central Bus (CTB) with 32-bit at 8MHz. Here, all the CPU, memory and I/O devices directly connect to the CTB.

2.5.8 PBus

Systems with PA-7000 or PA-7100/PA-7150 processors use the PBus processor bus between the CPU itself and the external memory controller (Viper). These system with VSC main bus mostly used ASP chipsets. On multi-processor systems with a PA-7100, two attachment variants were possible—either with a shared memory controller (two processors) or with a shared system bus (up to eight processors).

Bus features

- ◇ 32-bit multiplexed address/data bus
- ◇ Runs at fixed fractions of CPU clock (1.0, .67 and .50 of processor speed)
- ◇ Two multiprocessor strategies supported (only PA-7100; see below)

CPU attachment

1. **PBus** is the main processor and memory bus
 - ◇ CPU attaches to PBus with 32-bit
2. **Viper**, the main memory and I/O controller attaches to PBus
 - ◇ Memory attaches to MIOC via 72-bit (64-bit with ECC)
3. **VSC**, the system main bus, attaches to MIOC and various I/O controllers
 - ◇ Attaches via 32-bit (PA-7000) or 64-bit (PA-7100) at MIOC
4. I/O adapters attach to VSC
 - ◇ Either ASP chipset for SGC or GSC bus systems, or HP-PB adapters for some servers

Multiprocessor attachment

1. Two-way SMP (“Low Cost”): Two CPUs share a PBus and attach to the same MIOC. Memory attaches directly to MIOC, I/O attaches via VSC to MIOC.
2. Scalable MP: Each CPU has its own MIOC. All MIOCs in the system share a VSC bus, to which I/O and memory attach.

2.5.9 Runway

Runway is the system bus of newer 64-bit systems with PA-7200 and PA-8000 processors and up. It is a synchronous, split-transaction bus. PA-8500, PA-8600 and PA-8700 use an advanced version of Runway, Runway+/Runway DDR.

Bus features

- ◇ 64-bit multiplexed address/data
- ◇ 20 bus protocol signals
- ◇ Supports cache coherency
- ◇ Three frequency options (1.0, 0.75 and 0.67 of CPU clock — 0.50 apparently was later added)
- ◇ Parity protection on address/data and control signal
- ◇ Each attached device contains its own arbitrator logic
- ◇ Split transactions, up to six transactions can be pending at once
- ◇ Snooping cache coherency protocol
- ◇ 1-4 processors “glueless” multi-processing (no support chips needed)
- ◇ 768MB/s sustainable throughput, peak 960MB/s at 120MHz
- ◇ Runway+/Runway DDR: On PA-8500, PA-8600 and PA-8700, the bus operates in DDR (*double data rate*) mode, resulting in a peak bandwidth of about 2.0GB/s (Runway+ or Runway DDR) with 125MHz

Runway CPU attachments

The PA-7200, PA-8000 and PA-8200 processors with the Runway bus use split I/O and memory controllers—the U2/UTurn I/O Adapters (IOAs) and MMC/SMC memory controllers with each what can be called “frontends” and “backends”, with the former interfacing to the CPU and its processor bus and the latter attaching the frontend to customized bus attachments on their external side. This allowed HP to use the frontend parts of these chipsets with a variety of different system design which only required modified backend parts for new memory or I/O technologies.

1. **Runway** is the main processor and memory bus
 - ◇ 1-4 CPUs attach to Runway with 64-bit, parity-protected
 - ◇ SMP-capable
2. **MMC** is the main memory controller which attaches to Runway
 - ◇ Master Memory Controller (MMC)
 - ◇ Attaches to Runway with 64-bit (with example of 120MHz at a data rate of 960MB/s raw)
 - ◇ Memory attaches to MMC via slave Memory Controllers (SMC) and Data Multiplexers, 128-bit 60MHz data (ECC) and 39-bit 60MHz address buses
3. **U2/UTurn I/O adapters** attach the main I/O bus and system to the Runway processor bus

- ◇ Attach to Runway with 64-bit
 - ◇ Two I/O adapters (IOAs) per U2/UTurn chip
 - ◇ Maximum data rate depends on Runway clock with 120MHz and 64-bit: 960MB/s
4. **GSC+**, the main system bus, attach to the U2/UTurn IOAs
 - ◇ Attaches via 32-bit at a fraction of Runway/IOA clock, mostly 40MHz
 - ◇ PA-7300LC systems use the extended GSC version
 5. **I/O adapters and slots** attach to GSC+
 - ◇ LASI chipset
 - ◇ Video adapters
 - ◇ I/O slots extend GSC
 - ◇ Bus adapters, including EISA, VME and PCI, attach to GSC+

Runway+/Runway DDR CPU attachments

The PA-8500, PA-8600, PA-8700 processors use an advanced version of the Runway system bus with increased data rate and utilized different I/O and memory controllers, with most using the Astro chipset (IOMMU) and few servers the sophisticated Stretch and Cell chipsets.

Described below is the common configuration with Astro chipset—for the Stretch/Cell bus attachments see their entries at the Chipset page.

1. **Runway+/Runway DDR** is the main processor and memory bus
 - ◇ 1-4 CPUs attach to Runway with 64-bit, parity-protected
 - ◇ SMP-capable
2. **Astro** is the main memory and I/O controller which attaches to Runway
 - ◇ Attaches to Runway+/Runway DDR with 64-bit at maximum of 125MHz (with in this case 2.0GB/s peak data rate)
 - ◇ Memory attaches to Astro with a peak data rate of about 2.0GB/s at 125MHz
 - ◇ Up to eight I/O links (ropes) with each 250MB/s attach to Astro
3. **Elroy I/O adapters** attach PCI bridges via the I/O ropes to Astro
 - ◇ One or two ropes per Elroy PCI bridge
 - ◇ PCI slots or devices attach to Elroy bridges
4. **PCI**, the main I/O buses, attach to the multiple Elroy bridges
 - ◇ 33 or 66MHz, 32 or 64-bit
5. **I/O devices, adapters and slots** attach to PCI

References

1. **A High-Performance, Low-Cost Multiprocessor Bus for Workstations and Midrange Servers**⁸⁴
William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)

⁸⁴ <http://www.hpl.hp.com/hpjournal/96feb/feb96a2.pdf>

2.6 PA-RISC Graphics Adapters

2.6.1 Overview

All HP 32-bit and many of the earlier 64-bit PA-RISC computers used HP-designed video adapters, based on a variety of buses (GSC, SGC, etc.), chipsets and form factors. Only with the later PCI-based adapters HP switched to using customized versions of mainstream graphics adapters from the Intel/i386 world. The following sections describe most of the older, HP-proprietary designs.

2.6.2 CRX

CRX graphics adapters were available in various different configurations for both the GSG and GSC bus in their different formfactors. All of these adapters were officially only supported in HP-UX up to 10.20, some may still work with 11.00.

The CRX cards output a fixed resolution of 1280×1024. cards with SGC bus in the DIO-II formfactor use either one (grayscale), three (RGB) or four (RGB and sync) BNC connectors, while cards for SGC and GSC in the EISA formfactor and the mainboard-integrated CRX adapters use HD15 VGA connectors. *Multiple entries for one adapter list the different visuals which can be used when using HP's X11 server (i.e. under HP-UX with graphical interface).*

Table 2.8: HP CRX graphics adapters

Device	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Bus/Formfactor: Part-number
GRX	8-bit grayscale	1	-	software	-	SGC (DIO-II): A1924A
CRX	8-bit	2	-	hardware	-	SGC (DIO-II): A1659A
Stinger (CRX) <i>(See Note 1)</i>	8-bit	2	-	software	-	SGC (integrated)
Artist (CRX) <i>(See Note 2)</i>	8-bit	2	-	hardware	-	GSC (integrated)
CRX-24	8-bit	3	-	hardware	-	SGC (DIO-II FF): A1439A SGC (EISA FF): A2673A
	8-bit	3	8-bit	software	-	
	12-bit	1	-	hardware	-	
	24-bit	1	-	-	-	
CRX-24Z <i>(See Note 3)</i>	24-bit	1	-	-	yes	SGC (DIO-II FF): A1454A SGC (EISA FF): A2674A
CRX-48Z <i>(See Note 4)</i>	8-bit	1	-	hardware	-	SGC (DIO-II FF) + ext.: A2091A SGC (EISA FF) + ext.: A2675A GSC (EISA FF) + ext.: A4073A/B + A4074A
	8-bit	1	8-bit	software	-	
	24-bit	1	-	hardware	yes	

Notes

1. The *Stinger* CRX adapter, integrated into some of the older ASP-based workstations (older 715, 725), supports four different resolution/refresh-rate combinations, which can be changed via a DIP switch on the back of the machine or in the PDC.
2. The *Artist* graphics adapter, as found on many LASI-based workstations, is technically identical to the CRX devices but supports much more resolutions and refresh rates, which can be configured in the boot ROM.
3. The Z-suffix denotes a CRX board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (e.g. CRX-24Z) support the same visuals as stand-alone versions (e.g. CRX-24) but always provide the 3D acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

4. CRX-48Z adapters are GSC or SGC interface cards with a separate external processing box, which provides the RGB output connectors.

2.6.3 HCRX

The HCRX are the successors to the CRX graphics adapters and were shipped in systems with the GSC bus, either integrated into the mainboard or as a separate expansion board. They output a fixed resolution of 1280×1024 and use a HD15 VGA connector. *Multiple entries for one adapter list the different visuals which can be used when using HP's X11 server (ie. under HP-UX with a graphical interface).*

Table 2.9: HP HCRX graphics adapters

Device	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Bus/Formfactor: Part-number
HCRX-8	8-bit	2	-	hardware	-	GSC (EISA FF): A4070A/A4070B GSC (GSC-M FF): A4315A
HCRX-8Z (<i>See Note</i> 1)	8-bit	2 + 2 (ov.)	8-bit	software	-	
	8-bit	2	-	%	yes	GSC (EISA FF): A4079A/A4079B
HCRX-24	8-bit	2	-	hardware	-	GSC (EISA FF): A4071A/A4071B GSC (GSC-M FF): A4316A
	8-bit	2 + 2 (ov.)	8-bit	software	-	
	12-bit	1	-	hardware	-	
	24-bit	1	-	-	-	
HCRX-24Z (<i>See Note</i> 1)	24-bit	1	-	%	yes	GSC (EISA FF): A4179A

Notes

1. The Z-suffix denotes a HCRX-board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (e.g. HCRX-24Z) support the same visuals as stand-alone versions (e.g. HCRX-24) but always provide the 3D acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

2.6.4 Visualize

The HP Visualize line of graphics adapters were used in a large number of PA-RISC workstations integrated onto the mainboard and in expansion cards of various types. All cards provide 2D hardware acceleration, used by HP's X11 server on HP-UX. The 3D hardware acceleration is available in conjunction with either of the Starbase, PHIGS, PowerShade or PEX APIs.

The Visualize cards use either a HD15 VGA or EVC connector. *Multiple entries for one adapter list the different visuals which can be used when using HP's X11 server (ie. under HP-UX with a graphical interface).*

Table 2.10: HP Visualize graphics adapters

Device	max. resolution	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Bus/Formfactor: Part-number
Visualize-EG (base)	1280x1024	8-bit	2	-	software	-	GSC (EISA FF): A4450A GSC (HSC FF): A3519A PCI: A4977A PMC (PCI mezza- nine): A4979A
Visualize-EG (dual)	1280x1024	8-bit	2	-	software	-	GSC (EISA FF): A4451A
Visualize-EG (ext. mem)	1280x1024	8-bit	2 + 2 (ov.)	8-bit	software	-	GSC (EISA-FF): + A4452A
Visualize-8	1600x1200	8-bit	2	-	hardware	-	
	1280x1024	8-bit	2	-	hardware	yes	GSC (EISA FF): A4441A
		8-bit	2 + 2 (ov.)	8-bit	software	yes	
Visualize-24	1280x1024	8-bit	2	-	hardware	yes	GSC (EISA FF): A4442A
		8-bit	2 + 2 (ov.)	8-bit	software	yes	
		12-bit	1	-	hardware	yes	
		24-bit	1	-	-	yes	
Visualize-48	1280x1024	8-bit	4	-	hardware	yes	GSC (EISA FF): A4244A
		8-bit	4 + 2 (ov.)	8-bit	software	yes	
		24-bit	4	-	hardware	yes	
Visualize-4XP	1280x1024	8-bit	4	-	hardware	yes	GSC (2-slot EISA FF): A4246A GSC (HSC FF): A4455A
		8-bit	4 + 2 (ov.)	8-bit	software	yes	
		24-bit	4	-	hardware	yes	

2.6.5 Visualize-FX

The HP Visualize-FX graphics adapters were a more or less complete redesign in contrast to their Visualize predecessors. The architecture of the graphics processors is PA-RISC based, the higher-end models in fact include more than four PA-RISC CPUs to process the graphics. The FXs were the first HP cards to support the OpenGL X-Window Extension (GLX), in addition to the legacy 3D APIs (Starbase, PEX, PHIGS). These adapters were only available as PCI bus cards, with some using two slots.

The EVC connector present on some cards needs an adapter cable (about \$20) to connect to a HD15 VGA monitor.

These cards support a maximum resolution of 1600×1200 or 1280×1024 on older monitors. Both Sync-on-Green and Digital-Sync output signals are supported. *Multiple entries for one adapter list the different visuals which can be used when using HP's X11 server (ie. under HP-UX with a graphical interface).*

Table 2.11: HP Visualize-FX graphics adapters

Device	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Output	Bus/Formfactor: Part-number
Visualize-FXE	8-bit	2	-	hardware	yes	VGA	PCI 32-bit 66MHz: A4982A (See Note 1), A4982B (See Note 1)
	8-bit	2 + 2 (ov.)	8-bit	software	yes		
	24-bit	2	-	hardware	yes		
Visualize-FX2	8-bit	4	-	hardware	yes	EVC	PCI 64-bit 66MHz: A4552A
	8-bit	4 + 2 (ov.)	8-bit	software	yes		
	12-bit	2	-	hardware	yes		
	24-bit	4	-	-	yes		
Visualize-FX4/FX6 (See Note 2)	8-bit	4	-	hardware	yes	EVC	PCI 64-bit 66MHz: A4553A (FX4) PCI 64-bit 66MHz: A4554A (FX6)
	8-bit	4 + 2 (ov.)	8-bit	software	yes		
	12-bit	2	-	hardware	yes		
	24-bit	4	-	hardware	yes		
Visualize-FX5/FX10	8-bit	2	-	hardware	yes	VGA, DVI-D, stereo	PCI 64-bit 66MHz: A1264A (FX5) (See Note 3) PCI 64-bit 66MHz: A1264B (FX5pro) (See Note 3) PCI 64-bit 66MHz: A1298A (FX10) (See Note 3) PCI 64-bit 66MHz: A1298B (FX10pro) (See Note 3)
	8-bit	2 + 2 (ov.)	8-bit	software	yes		
	24-bit	2	-	hardware	yes		

Notes

1. Two different FXE models with different memory subsystems were shipped:
 - ◇ A4982A: 18MB SGRAM, (3.5MB max for textures)
 - ◇ A4982B: 24MB SDRAM, (9.5MB max for textures)The A-version is slightly faster due to the use of SGRAM.
2. The FX4 and FX6 cards support an optional 16MB hardware texture memory module.
3. The FX5/10pro models integrate the raster and texture-processor onto a single chip, resulting in a better performance than the standard FX5/10 models. The onboard RAM is used as unified buffer, Z-buffer and texture storage:
 - ◇ FX5[pro]: 64MB (48MB max. for textures)
 - ◇ FX10[pro]: 128MB (110MB max. for textures)

2.6.6 FireGL-UX

The FireGL-UX high-end graphics adapter was based on ATI's FireGL2 board, often used in Intel i386 PCs. It provides full OpenGL hardware acceleration under HP's X server and is binary compatible with the Visualize FX1opro adapter.

Details:

- ◇ IBM GT1000 geometry engine
- ◇ IBM RC1000 raster engine
- ◇ 128MB DDR SDRAM of unified frame buffer, Z-buffer and texture storage
- ◇ Digital DVI and 3-pin stereo output
- ◇ 64-bit, 66MHz PCI card

It is about twice as fast as the Visualize FX1opro.

Supported resolutions and refresh rates:

Table 2.12: HP FireGL-UX graphics adapter supported resolutions

Resolution	Refresh rate	Color depth
640×480	100Hz	24-bit
800×600	100Hz	24-bit
1024×768	100Hz	24-bit
1152×864	100Hz	24-bit
1280×960	100Hz	24-bit
1280×1024	100Hz	24-bit
1600×1000	85Hz	24-bit
1600×1024	85Hz	24-bit
1600×1200	85Hz	24-bit
1792×1344	60Hz	24-bit
1920×1200	76Hz	24-bit

2.6.7 References

- ◇ HP-UX Graphics Administration Guide⁸⁵

⁸⁵ <http://docs.hp.com/hpux/onlinedocs/B2355-90142/B2355-90142.html>

2.7 PA-RISC SCSI

2.7.1 SCSI bus

The below table lists some variants of the SCSI bus as found in PA-RISC computers.

Table 2.13: SCSI buses in PA-RISC computers

SCSI	Clock	Width	Data rate (max)	Devices (max) (See Note 1)	Signals (See Note 2)	Length (max)	Connector
Narrow SCSI	5MHz	8-bit	5MB/s	7	SE	6m	50-pin
Fast-Narrow SCSI	10MHz	8-bit	10MB/s	7	SE	3m	50-pin
					HVD	2.5m	
Fast-Wide SCSI	10MHz	16-bit	20MB/s	15	SE	3m	68-pin
					HVD	2.5m	
Ultra-Narrow SCSI	20MHz	8-bit	20MB/s	7	SE	1.5m	50-pin
					LVD	1.2m	
					HVD	2.5m	
Ultra-Wide SCSI	20MHz	16-bit	40MB/s	15	SE	1.5m	68-pin
					LVD	1.2m	
					HVD	2.5m	
Ultra2-Wide SCSI	40MHz	16-bit	80MB/s	15	LVD	1.2m	68-pin
Ultra160 SCSI	40MHz	16-bit	160MB/s	15	LVD	1.2m	68-pin
Ultra320 SCSI	80MHz	16-bit	320MB/s	15	LVD	1.2m	68-pin

Notes

1. Excluding the SCSI controller
2. Signalling:
 - ◇ SE - Single-Ended
 - ◇ HVD - High-Voltage Differential
 - ◇ LVD - Low-Voltage Differential

2.7.2 SCSI chipsets

A listing of the common SCSI chipsets used in some of the PA-RISC workstations and servers from HP. These chips were both integrated into the main logic of these systems or available on plug-in cards.

53C700

Used in

- ◇ 705, 710, 715, 720, 730, 750, 725 735, 755 (ASP2)

- ◇ 742i, 745i, 747i

The 53C700 is the primary SCSI controller of the very early PA-RISC workstations which include the ASP chipset. It only supports 5MHz narrow-transfers.

Features

- ◇ One narrow SCSI channel
- ◇ Chip support for SE transfer modes
- ◇ Synchronous SCSI transfer rate of 5MB/s

53C710

Used in

- ◇ 712, 715, 725
- ◇ 743i, 744, 745, 748i
- ◇ A180, A180C
- ◇ B132L, B132L+, B160L, B180L+
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- ◇ D-Class
- ◇ E25, E35, E45, E55
- ◇ J200, J210, J210XC, J280, J282
- ◇ K-Class
- ◇ RDI PrecisionBook 132, 160, 180
- ◇ R380, R390
- ◇ SAIC Galaxy 1100

The NCR 53C710 was the primary SCSI controller used in the early, post-ASP HP 9000s. Integrated in the LASI ASIC as a macrocell, all of the above named workstations used this implementation as the controller for their 8-bit SE SCSI-2 bus.

Features

- ◇ One Fast-Narrow SCSI channel
- ◇ Chip support for SE and HVD transfer modes (in the HP 9000s only SE logic is used)
- ◇ Synchronous SCSI transfer rate of 10MB/s
- ◇ Asynchronous SCSI transfer rate of over 5MB/s
- ◇ 64-Byte DMA FIFO
- ◇ Bus master DMA device

- ◇ Attaches to host bus interface, can either be Motorola 68030 (bus up to 25MHz async) or 68040 (bus up to 33MHz sync) compatible
- ◇ Sustained host bus bandwidth of up to 42.66MB/s

53C720

Used in

- ◇ 735, 755 (ASP2)
- ◇ B132L, B160L
- ◇ C100, C110, C132L, C160L, C160, C180
- ◇ D-Class
- ◇ J200, J210, J210XC, J280, J282
- ◇ K-Class
- ◇ R380, R390

The NCR 53C720 was the secondary SCSI controller used in the early HP 9000s for the attachment of an Fast-Wide (16-bit) SCSI-2 bus, utilizing HVD signalling. It was either controlled by the ASP2 chipset or interfaced to the GSC bus through a chip named Zalon.

Features

- ◇ One Fast-Wide SCSI channel
- ◇ Chip support for SE and HVD transfer modes (in the HP 9000s only HVD logic is used)
- ◇ Synchronous SCSI transfer rate of 20MB/s
- ◇ Asynchronous SCSI transfer rate of 10MB/s
- ◇ 64-Byte DMA FIFO
- ◇ 16- or 32-bit bus master DMA device
- ◇ Attaches to host bus interface, can either be Motorola 68030 (bus up to 25MHz async) or 68040 (bus up to 33MHz sync) or Intel 80386SX or 80386DX compatible
- ◇ Support both big or little endian
- ◇ Sustained host bus bandwidth of more than 100MB/s
- ◇ 208-pin QFP package

53C875

Used in

- ◇ A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- ◇ B132L+, B180L+
- ◇ C200, C240, C360

- ◇ L1000 (rp5400), L2000 (rp5450)
- ◇ N4000
- ◇ Superdome
- ◇ V2200, V2250

The Symbios Logic/LSI 53C875 is the chip that provides the single Ultra-Wide SE SCSI channel on some of the newer PA-RISC workstations.

Features

- ◇ One Ultra-Wide SCSI channel
- ◇ Chip support for SE transfer modes
- ◇ Synchronous SCSI transfer rate of 40MB/s
- ◇ Asynchronous SCSI transfer rate of 14MB/s
- ◇ 4KB SCRIPTS RAM
- ◇ 536-Byte DMA FIFO
- ◇ 20MHz SCSI clock
- ◇ Attaches to 32-bit, 33MHz PCI (PCI-32/33), both 3.3V or 5V
- ◇ 160-pin PQFP or 169-pin PBGA package

References

- ◇ LSI 53C875E⁸⁶ (PDF, 0.3MB)

53C896

Used in

- ◇ A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- ◇ B1000, B2000, B2600
- ◇ C3000, C3600, C3700
- ◇ J5000, J5600, J6000, J6700, J7000, J7600
- ◇ L1000 (rp5400), L2000 (rp5450)

The Symbios Logic 53C896 SCSI ASIC is the chip used on some of the newer PA-RISC workstations and servers to control their storage I/O buses. This ASIC includes two 53C895-equivalent cores to control the two internal channels separately.

⁸⁶ http://www.lsilogic.com/files/docs/marketing_docs/storage_stand_prod/raid/lsi53c875e_pb.pdf

Features

- ◇ Two independent Ultra2-Wide SCSI-3 channels
- ◇ Chip support for LVD, HVD and SE transfer modes
- ◇ Synchronous SCSI transfer rate of 80MB/s for each channel
- ◇ Integrated LVDlink SCSI transceivers
- ◇ 8KB SCRIPTS RAM for each channel
- ◇ 944-Byte DMA FIFO for each channel
- ◇ 40MHz SCSI clock
- ◇ Attaches to 64-bit, 33MHz PCI (PCI-64/33)
- ◇ 329-pin PBGA package

References

- ◇ LSI 53C896⁸⁷ (PDF, 0.2MB)

2.7.3 SCSI Adapters

SCSI adapters (HBAs) for the various expansion buses found in PA-RISC systems.

EISA

SCSI adapters for the EISA bus.

Table 2.14: EISA SCSI adapters for PA-RISC computers

Part-no.	SCSI type	Signalling (<i>See Note 1</i>)	Boot	HP-UX
A2679A	Fast-Narrow	SE	no	9.0-11i/32-bit
25525A	Fast-Narrow	HVD		8.05-10.20
25525B	Fast-Narrow	HVD		8.05-11.0/32-bit

GSC

SCSI adapters for the variants of the GSC bus.

Table 2.15: GSC SCSI adapters for PA-RISC computers

Part-no.	GSC formfactor	SCSI type	Signalling (<i>See Note 1</i>)	Boot	HP-UX
A2874-66005	EISA	Fast-Wide	HVD	yes	9.05/11.0
A2969A	HSC	Fast-Wide	HVD	yes	10.01-11i
A3644A (<i>See Note 2</i>)	HSC	Fast-Wide	HVD		10.20-11i
A4107A	EISA	Fast-Wide	HVD		9.05-11i/32-bit
A4268A	GSC-M	Fast-Wide	HVD	yes	9.05-11.0/32-bit

⁸⁷ http://www.lsillogic.com/files/docs/marketing_docs/storage_stand_prod/raid/lsi53c896_pb.pdf

HP-PB

SCSI adapters for the HP-PB bus.

Table 2.16: HP-PB SCSI adapters for PA-RISC computers

Part-no.	SCSI type	Signalling (<i>See Note 1</i>)	Boot	HP-UX
27251A				
28655A	Fast-Narrow	SE	yes	10.01-11i
28696A	Fast-Wide	HVD	yes	10.01-11i

PCI

SCSI adapters for the PCI bus.

Table 2.17: PCI SCSI adapters for PA-RISC computers

Part-no.	SCSI type	Signalling (<i>See Note 1</i>)	Boot	HP-UX
A4800A	Fast-Wide	HVD	yes	10.2-11i
A4974A	Ultra-Wide	SE	yes	10.20-11.0
A4976A	Fast-Wide	HVD	yes	10.20-11.0
A4999A	Ultra2-Wide	LVD	yes	10.20-11.0
A5159A	Fast-Wide	HVD	yes	10.20-11i

Notes

1. Signalling:
 - ◇ SE - Single-Ended
 - ◇ HVD - High-Voltage Differential
 - ◇ LVD - Low-Voltage Differential
2. This card is only supported in the T-Class

Chapter 3

PA-RISC Operating Systems

3.1 Overview

A broad range of operating systems is available for PA-RISC workstations and, to a lesser extent, servers. They are either Unix or Unix-like, with different designs having both been ported to and developed specifically for PA-RISC, including open source, research and commercial products. Most of the earlier efforts were distributed only to a small, academic circle and not available to the general public. The current open-source projects are available freely together with sources to the general public.

3.1.1 Commercial products

Few commercial operating systems support PA-RISC computers, with the most prominent Unix systems being HP-UX and NeXTSTEP. (HP also sells a real-time system for the HP 9000, HP-RT, not discussed here.)

HP-UX is HP's own Unix version for PA-RISC computers. All PA-RISC computers from HP are supported by different versions of HP-UX.

NeXTSTEP is an operating system based on a Mach microkernel with an Unix userland and a slick GUI, released for PA-RISC in 1994. Support for some 32-bit PA-RISC machines was available in Version 3.3, with limited hardware support.

3.1.2 Open Source projects

Several open source operating systems support the PA-RISC architecture, including Linux, OpenBSD and NetBSD. They are all Unix-like.

PA-RISC Linux supports different machines from the newer 32 and 64-bit series though proper support is still missing for a lot of systems. Linux does not perform equally well as original HP-UX on PA-RISC systems and hardware support is limited.

OpenBSD/hppa supports most 32-bit systems, and some 64-bit systems in 32-bit mode. Newer machines running in full 64-bit mode are not supported and later will supposedly be by OpenBSD/hppa64.

NetBSD supports several 32-bit machines, with support for newer machines ported over from OpenBSD. NetBSD/hp700 is not a major NetBSD effort; it supports some systems and most of the hardware OpenBSD/hppa supports.

3.1.3 Research projects

Various research operating systems were ported to PA-RISC at different places over the time. All of these systems were BSD/Unix operating systems based mostly on the Mach microkernel. The ports were mostly development or research projects, and not operating systems releases in the formal sense. Many were developed at the University of Utah and later formed the starting point for PA-RISC ports of other operating systems (OpenBSD, Linux).

These ports include HPBSD, Mach-based Unix/BSD systems, Chorus, OSF/1 ports and MkLinux.

3.2 HP-UX

3.2.1 Overview

HP-UX is HP's[†] Unix operating system. First released in 1986 on the HP 9000/500 series with HP FOCUS CPUs, HP-UX in its current version 11i runs on most PA-RISC 1.1 and 2.0 and Itanium 2 computers from HP.

Until version 9.x HP-UX had very strong BSD Unix influences (and supposedly was very close to HPBSD); from versions 10.x onward it became more close to the System V line of Unix (SVR4). The PA-RISC version of HP-UX including 10.20 were split into different releases for *workstations* (HP 9000/700) and *servers* (800). HP-UX 10.20 was quite popular, since it ran very smoothly on older systems and had support for most available PA-RISC hardware.

From HP-UX 11.00 onward, unified releases were made for servers and workstations (700s and 800s). The 11 line of HP-UX was the first complete 64-bit version with support for the 64-bit features 64-bit PA-8x00 processors.

3.2.2 HP-UX 10.20

HP-UX 10.20 is quite fast on all supported machines with at least 64MB RAM. Most administration tasks can be done using the **sam** system administration manager: *e.g.*, adding devices, configuring the kernel, X server, network and mounting filesystems.

Different releases were made for HP 9000/700 workstations and the HP 9000/800 servers.

System requirements

- ◇ Most available 32-bit workstations and servers are supported.
- ◇ Many 64-bit systems are supported, however only older ones. However, versions 11.x are a better fit for these systems.
- ◇ About 300-800MB disk space required.
- ◇ 64MB RAM minimum, 128MB or more better
- ◇ All available HP graphics options are supported
- ◇ All available HP input devices are supported
- ◇ Most networking and other I/O adapters supported

Supported systems

- ◇ 705, 710, 712, 715, 720, 730, 750, 725, 735, 755
- ◇ 742i, 743i, 744, 745i, 745, 747i, 748i, 748
- ◇ A180, A180C
- ◇ B132L, B160L, B132L+, B180L+, B1000, B2000

[†] <http://www.hp.com>

- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600
- ◇ D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
- ◇ E25, E35, E45, E55
- ◇ J200, J210, J280, J282, J2240, J5000, J5600, J6000, J7000
- ◇ K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
- ◇ Nova servers (F, G, H, I-Class)
- ◇ R380, R390
- ◇ RDI PrecisionBook
- ◇ SAIC Galaxy 1100

3.2.3 HP-UX 11.00

Version 11.00 is HP's first Unix to implement a full 64-bit kernel. Nevertheless, it still runs on a number of systems featuring a 32-bit CPU. All HP 9000/800 servers with at least a PA-7000 should be supported, although some expansion options have been discontinued for those systems. *Official* support for HP 9000/700 workstations was only continued for those systems featuring at least a PA-7100LC CPU. With careful review of the newer OS patches older systems with *e.g.*, PA-7100 and PA-7150 CPUs can also be made to run 11.00.

11.00 can run in either 64-bit or 32-bit mode on systems with a PA2.0 processor (i.e. at least PA-8000) or in 32-bit mode on all PA1.1 processors.

System requirements

- ◇ Needs minimum 500MB to 1GB diskspace
- ◇ At least 128MB of RAM; more than 256MB is much better
- ◇ All available HP input devices supported
- ◇ GRX and CRX (CRX-8, [H]CRX-24[Z], [H]CRX-48-[Z] frame buffers not supported
- ◇ Several EISA expansion cards and all HP-IB interfaces not supported

Supported systems

- ◇ Officially unsupported but could run: 705, 710, 720, 730, 750, 735, 755, 745i, 747i,
- ◇ 712, 715 (some unsupported), 725 (some unsupported), 743i, 744, 745, 748, 748i
- ◇ A180, A180C, A400 (rp2400/rp2430), A500 (rp2450/rp2470)
- ◇ B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3650, C3700, C3750
- ◇ D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390

- ◇ E25, E35, E45, E55
- ◇ J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000
- ◇ K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
- ◇ L1000 (rp5400), L2000 (rp5450), L1500 (rp5430), L3000 (rp5470) (L1500 unsure/unsupported)
- ◇ N4000 (rp7400), N4000 (rp7405/rp7410) (the last two: unsure/unsupported)
- ◇ Nova servers (F, G, H, I-Class)
- ◇ R380, R390
- ◇ RDI PrecisionBook
- ◇ SAIC Galaxy 1100
- ◇ T500, T520, T600
- ◇ V2200, V2250, V2500, V2600

3.2.4 HP-UX 11i (11.11)

Version 11i (or 11.11) is the latest HP-UX release for PA-RISC based computers and extends the hardware support from 11.00 to more high-end systems as *e.g.*, SuperDome featuring up to 128 CPUs. As this is the current active HP-UX release most patches and available software are geared towards 11i. The 11i CD sets were/are made available bi-annually, newer releases always include current patch sets and software enhancements.

There are different versions of HP-UX 11i targeting different system families:

- ◇ HP-UX 11i v1: the original release supporting most 64-bit PA-RISC systems and many older 32-bit servers and workstations. Some even older 32-bit PA-RISC systems were officially unsupported but could be made to work with some v1 releases.
- ◇ HP-UX 11i v1.5 and v1.6: special version supporting the first generation Itanium and several early Itanium 2 systems
- ◇ HP-UX 11i v2: supports the later 64-bit PA-RISC servers (with *rp*-designations) and Itanium 2 servers and workstations
- ◇ HP-UX 11i v3: similar to v2 but supporting only the latest 64-bit PA-RISC servers and Itanium 2 servers

System requirements

The list of officially supported systems was reduced even further compared to 11.00, with support for older systems was phased out. In some cases officially unsupported systems can run 11i, though with a sometimes complicated installation and careful review of operating systems patches afterward. Since patches are generally shipped with newer versions, older systems need older HP-UX installation releases (CDs).

11i generally has the same requirements as 11.00, although 256MB of RAM should be the minimum for a graphical environment.

Support for several I/O subsystems and devices ended with 11i—this includes various networking, graphics and bus adapters (see the release notes for exact information). EISA is generally unsupported with 64-bit 11i.

HP-UX 11i v1 supported systems

- ◇ 735, 755 (officially unsupported)
- ◇ 712, 715/64/80/100/100XC, 725/100, 743i, 744, 745, 748, 748i (all last release v1 December 2004)
- ◇ A180, A180C, A400 (rp2400/rp2430), A500 (rp2450/rp2470)
- ◇ B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3650, C3700, C3750
- ◇ D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
- ◇ E25, E35, E45, E55 (officially unsupported)
- ◇ J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000
- ◇ K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
- ◇ L1000 (rp5400), L2000 (rp5450), L1500 (rp5430), L3000 (rp5470)
- ◇ N4000 (rp7400), N4000 (rp7405/rp7410)
- ◇ rp3410, rp3440, rp4410, rp4440, rp7420, rp7440, rp8400, rp8420, rp8440
- ◇ Nova servers (F, G, H, I-Class) (officially unsupported)
- ◇ R380, R390
- ◇ RDI PrecisionBook
- ◇ SAIC Galaxy 1100
- ◇ T500, T520, T600
- ◇ V2200, V2250, V2500, V2600
- ◇ Superdome PA-RISC models

HP-UX 11i v2 supported systems

- ◇ A400 (rp2400/rp2430), A500 (rp2450/rp2470)
- ◇ L1000 (rp5400), L2000 (rp5450), L1500 (rp5430), L3000 (rp5470)
- ◇ N4000 (rp7400), N4000 (rp7405/rp7410)
- ◇ rp3410, rp3440, rp4410, rp4440, rp7420, rp7440, rp8400, rp8420, rp8440
- ◇ rx1600, rx1620, rx2600, rx2620, rx2660, rx3600, rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640

- ◇ Superdome
- ◇ zx2000, zx6000 (both v2 May 2005 last)

HP-UX 11i v3 supported systems

- ◇ N4000 (rp7400), N4000 (rp7405/rp7410)
- ◇ rp3410, rp3440, rp4410, rp4440, rp7420, rp7440, rp8400, rp8420, rp8440
- ◇ rx1600, rx1620, rx2600, rx2620, rx2660, rx3600, rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
- ◇ Superdome

3.2.5 Software for HP-UX

Repositories

- ◇ **Software Porting And Archive Centre for HP-UX²**, compiled software packages (open source) for both HP-UX 10.20 and 11
- ◇ **The Written Word FTP³**, selected software for HP-UX 10.20
- ◇ **The Written Word FTP⁴** for HP-UX 11
- ◇ **HP software depot⁵**, software packages from different categories for download (mostly free of charge), from HP

Documentation

- ◇ **HP DSPP developer edge⁶**, resources for HP-UX developers
- ◇ **Managing HP-UX Software With SD-UX⁷** Hewlett-Packard Company (November 1997: accessed January 2009)

3.2.6 Further reading

Manuals

- ◇ **HP-UX 11i Version 1 Installation and Update Guide: HP Servers and Workstations⁸** Hewlett-Packard Company (June 2004: accessed January 2009. HP part number 5990-7279)
- ◇ **Installing HP-UX 11.0 and Updating HP-UX 10.x to 11.0: HP 9000 Computers⁹** Hewlett-Packard Company (November 1997: accessed January 2009. HP part number B2355-90153)

² <http://hpux.asknet.de>

³ <ftp://ftp.thewrittenword.com/packages/by-architecture/hppa1.1-hp-hpux10.20/>

⁴ <ftp://ftp.thewrittenword.com/packages/by-architecture/hppa1.1-hp-hpux11.00/>

⁵ <http://www.software.hp.com/>

⁶ <http://h21007.www2.hp.com/dev/>

⁷ http://www.docs.hp.com/hpux/onlinedocs/B2355-90154/B2355-90154_top.html

⁸ <http://docs.hp.com/hpux/onlinedocs/5990-7279/5990-7279.html>

⁹ <http://docs.hp.com/hpux/onlinedocs/B2355-90153/B2355-90153.html>

- ◇ **Installing and Updating HP-UX 10.20, ACE and Hardware Extensions: HP 9000 Computers**¹⁰ Hewlett-Packard Company (April 1998: accessed January 2009. HP part number B2355-90173)
- ◇ **HP-UX manual pages**¹¹ Hewlett-Packard Development Company (2009: accessed January 2009)

Websites

- ◇ **HP-UX update matrix**¹² (HP-UX 11.x support for workstations) Hewlett-Packard Development Company (2009: accessed January 2009)
- ◇ **HP-UX server support matrix**¹³ (.pdf) (HP-UX 11.x support for servers) Hewlett-Packard Development Company (November 2008: accessed January 2009)
- ◇ **HP-UX update matrix**¹⁴ (archive.org mirror) (HP-UX 10.20 and 11.x support for workstations) Hewlett-Packard Development Company (2003: accessed March 2009)
- ◇ **HP-UX version and server model support matrix**¹⁵ (archive.org mirror) (HP-UX 11 support for servers) Hewlett-Packard Company (2001: accessed April 2009)
- ◇ *Building a Bastion Host Using HP-UX 11*, Kevin Steves (April 2000: Hewlett-Packard Sweden) [used to be available from HP, now can be found on various places — *Ed.*]
- ◇ **docs.hp.com - Technical documentation**¹⁶, good entry to HP/HP-UX documentation

Release notes

- ◇ **HP-UX 11i v3 Release Notes**¹⁷ (docs.hp.com)
- ◇ **HP-UX 11i v2 Release Notes**¹⁸ (docs.hp.com)
- ◇ **HP-UX 11i v11.5 Release Notes**¹⁹ (docs.hp.com)
- ◇ **HP-UX 11i v1 Release Notes**²⁰ (docs.hp.com)

Other documents

- ◇ **HP-UX FAQ**²¹ (comp.sys.hp.hpux FAQ) Ian Springer (February 2008: accessed January 2009)
- ◇ **INFORMATION ON HP9000 SERVERS AND WORKSTATIONS**²² Hewlett Packard Company (1997 (1999): accessed January 2009)

¹⁰ <http://docs.hp.com/hpux/onlinedocs/B2355-90173/B2355-90173.html>

¹¹ http://www.docs.hp.com/hpux/os/man_pages.html

¹² http://www.hp.com/workstations/risc/standard/operating/support_matrix/update.html

¹³ http://h20338.www2.hp.com/hpux11/downloads/public_hp-ux_systems_support.pdf

¹⁴ http://web.archive.org/web/20041205072423/http://www.hp.com/workstations/risc/standard/operating/support_matrix/update.html

¹⁵ <http://web.archive.org/web/20011101160143/http://devresource.hp.com/STK/serversupport.html>

¹⁶ <http://docs.hp.com>

¹⁷ <http://docs.hp.com/en/oshpux11iv3.html#ReleaseNotes>

¹⁸ <http://docs.hp.com/en/oshpux11iv2.html#ReleaseNotes>

¹⁹ <http://docs.hp.com/en/hpuxos11iv1.5.html#ReleaseNotes>

²⁰ <http://docs.hp.com/en/oshpux11i.html#ReleaseNotes>

²¹ <ftp://rtfm.mit.edu/pub/faqs/hp/hpux-faq>

²² http://www.parisc-linux.org/documentation/hp9000_models.html

3.3 PA-RISC Linux

3.3.1 Overview

The **PA-RISC Linux**²³ port runs on a broad range of both 32-bit and 64-bit workstations and servers.

Most of the “unlettered” (the HP 9000/700s) and B/C/J-Class workstations are supported, both 32-bit (based on PA-7x00 processors) and 64-bit (PA-8x00) systems in the same distribution. SMP is supported, though not as smooth as on other Linux platforms or HP-UX and not necessarily with the theoretical maximum of CPUs. PA-RISC Linux runs on most server systems, although several which use proprietary I/O and CPU/memory combinations are unsupported.

Originally started by “The Puffin Group” in 1998, the port of **Linux**²⁴ to HP PA-RISC gained momentum after HP started helping with equipment and more importantly, documentation, in 1999 and quickly superseded the earlier Mach-based MkLinux. Because of HP’s assistance, the machines targeted at that time were newer than what other ports (*e.g.*, OpenBSD or MkLinux) supported, like the A180, B180 and 64-bit PA 2.0 systems. Nevertheless, PA-RISC Linux also supports older HP 9000/700 systems like 712, 715 and 735.

3.3.2 Supported systems

- ◇ 705, 710, 712, 715, 720, 730, 750, 725, 735, 755
- ◇ 742i, 743i, 744, 745i, 745, 747i 748i, 748
- ◇ A180, A180C, A400 (rp2400/rp2430), A500 (rp2450/rp2470)
- ◇ B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3650, C3700, C3750
- ◇ D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
- ◇ E-Class (very limited support)
- ◇ J200, J210[XC], J280, J282, J2240, J5000, J6000, J6700, J7000
- ◇ K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
- ◇ L1000 (rp5400), L2000 (rp5450), L3000 (rp5470)
- ◇ N4000 (rp7400)
- ◇ R380, R390
- ◇ RDI PrecisionBook
- ◇ SAIC Galaxy 1100

Performance is not quite on par with original HP-UX—50% is a fair rough estimate of the relative raw performance, although the overhead of a complete running HP-UX probably consumes much of this advantage, especially on older systems.

²³ <http://www.parisc-linux.org>

²⁴ <http://www.kernel.org>

3.3.3 Supported hardware

Most I/O subsystems are supported, including many common PC expansion possibilities. Correct X11 graphical support is limited to a small set of HP adapters via the framebuffer device. As the newer machines are more similar to standard Intel PCs, support is generally better but still lacking in some areas.

3.3.4 Development

In the late 1990s PA-RISC was the last “big” RISC/Unix architecture without a proper Linux port, besides the limited useful Mach-based MkLinux. This had multiple reasons, including that PA-RISC systems were not widely used in academia with a stronger market share in the technical/industrial space, from which they did no escape for a long time. Another reason was HP only reluctantly releasing technical documentation on their systems to the public, which limited interest in and progress of development efforts.

A function of the confinement to the industry was a limited hobbyist base for PA-RISC as the available machines were not well documented and did not have proper operating systems for private users, as compared to *e.g.*, the more popular Sun SPARC systems. Slow progress was made in 1999 with the initial start of the original Linux kernel on PA-RISC, as there was growing interest in these machines (when more made their way into the second-hand market), and finally more and more documentation was released.

PA-RISC Linux/Puffingroup

The primary center of kernel and toolchain development is the official **PA-RISC Linux project**²⁵. A range of resources is provided, including access to the source code, mailing lists for users and developers, installation instructions, an array of documentation and a hardware database.

Early work started in 1999 with the help of The Puffin Group, later employing several kernel and toolchain developers. Development was at first directed towards 32-bit systems; later on, with the help of Hewlett Packard, more modern machines were made available to developers, resulting in generally broader hardware and 64-bit support. Several important parts of the kernel PA-RISC support were written by HP employees participating in the project. The PA-RISC Linux affiliations changed throughout the last years, HP and developer support fluctuated but the port reached a stable state.

ESIEE

(Contributed by Thibaut Varene)

The PA-RISC Linux port effort started at ESIEE²⁶ in December 1999, with Thierry Simonnet (who was then managing the General IT Resources Service at ESIEE) getting involved in the early stages of the port. By mid September 2000, Simonnet decided to get students involved, and he started a case study for students to participate in as part of their school curriculum. The study was conducted in parallel by HP Labs, who massively sponsored the effort of the school, being one of its long time key partner. This enabled the students to rapidly acquire skills and credibility, and the study was completed in February 2001, and presented at Linux Expo in Paris, and several months later at the Debian 1 Conference in

²⁵ <http://www.parisc-linux.org>

²⁶ <http://www.esiee.fr>

Bordeaux, France. With its increasing success, the initial case study spawned into a larger project that was open to students either on their free time or as part of their classes, and more of them joined what was to be called the PATeam. From 2001 to the end of 2003, the team has been very active, doing numbers of development in the Linux kernel (writing drivers and improving overall stability).

Unfortunately, in 2004 and thereafter, ESIEE gradually reduced its support for the project, and nowadays it doesn't support it anymore, save for website and machines hosting.

3.3.5 Distributions

Since late 2005 there are two popular Linux distributions that include the PA-RISC port: Debian and Gentoo.

Debian

Debian²⁷ includes PA-RISC Linux as **Debian/hppa**²⁸ in various releases, including 4.0 ("Etch"), 3.1 ("Sarge") and 3.0 ("Woody"). CDs can be ordered as media or downloaded as ISO images from **Debian FTP mirrors**²⁹ in the 4.0_*/hppa (or 3.1_*/hppa or 3.0_*/hppa) directories.

Gentoo

Gentoo³⁰ was the second distribution which included a **PA-RISC port**³¹. Gentoo is completely compiled from source and uses a BSD-style ports system.

3.3.6 References

Documentation

- ◇ **PA-RISC Linux: HARDWARE SUPPORT**³² The PARISC-Linux Project (December 2005. Accessed January 2009)
- ◇ **ESIEE PA/Linux Detailed Hardware Support**³³ ESIEE The PA/Linux Team (January 2007. Accessed January 2009)
- ◇ **PA-RISC Linux hardware database**³⁴ The PARISC-Linux Project (June 2007. Accessed January 2009)

Websites

- ◇ **PA-RISC Linux project page**³⁵ The PARISC-Linux Project (December 2008. Accessed January 2009)

²⁷ <http://www.debian.org/>

²⁸ <http://www.debian.org/ports/hppa/>

²⁹ <http://ftp.ie.debian.org/debian-cd/>

³⁰ <http://www.gentoo.org>

³¹ <http://www.gentoo.org/doc/en/handbook/handbook-hppa.xml>

³² <http://www.parisc-linux.org/hardware/supported.html>

³³ <http://www.pateam.org/list.html>

³⁴ <http://hwdb.parisc-linux.org>

³⁵ <http://www.parisc-linux.org>

- ◇ ESIEE PA/Linux project page³⁶ ESIEE The PA/Linux Team (2007. Accessed January 2009)

Other documents

- ◇ Linux on PA-RISC. One Martini Too Many³⁷ (.pdf) Matthew Wilcox (July 2000: Paper for OLS2000)

³⁶ <http://www.pateam.org>

³⁷ <http://ftp.parisc-linux.org/docs/willy/ols2.pdf>

3.4 NetBSD/hp700

3.4.1 Overview

NetBSD is a free, open source Unix-like operating system, and has support for PA-RISC 1.1 systems in its NetBSD/hp700³⁸ port since 2004/2005. It is a variant of BSD Unix and a descendant of 4.3BSD, from which it emerged in 1993 via the free 386BSD and Networking/2 releases. NetBSD/hp700 is available via binary snapshots, since the PA-RISC port never reached the status of a formal release version.

Work on a port to 32-bit PA-RISC systems was started several times during the 1990s and early 2000s. The current effort is largely based on Michael Shalayeff's work on the OpenBSD/hppa kernel from 2004 to 2005, from which NetBSD/hp700 used many parts.

The port focuses on 32-bit PA-RISC 1.1 computers based on PA-7100, PA-7100LC and PA-7300LC processors.

NetBSD/hp700 is the least complete port of the three current open source systems, trailing both Linux and OpenBSD on PA-RISC.

3.4.2 Supported systems

- ◇ 712, 715, 725, 735, 755
- ◇ A180[C]
- ◇ B132L, B160L, B132L+, B180L+
- ◇ C132L, C160L
- ◇ D220, D230, D320, D330
- ◇ RDI PrecisionBook

3.4.3 Supported hardware

Buses and chipsets

PCI and GSC buses and onboard bus controllers (ASP, LASI, Dino/Cujo) are supported.

ISA/EISA, Cardbus and HP-PB buses and bus controllers are not supported.

Networking

All on-board Ethernet and Fast-Ethernet network interfaces are supported; the FDDI sliders on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel i8255x, Realtek 8120/8139, NE2000, SiS 900) could work. No other network expansion boards (ATM, FDDI, Gigabit Ethernet) are supported.

Realtek RTL8150L USB-based Ethernet adapters are supported.

³⁸ <http://www.netbsd.org/Ports/hp700/>

Storage

Storage I/O is supported via the NCR 53C700 narrow, NCR 53C710 Fast-Narrow or NCR 53C875 Ultra-Wide SE SCSI controllers. The on-board NCR 53C720 Fast-Wide HVD controllers are not supported.

GSC/HSC and PCI expansion cards with one of the 53C710 or 53C8xx (siop) SCSI chipsets, Adaptec 2940 (ahc) PCI and various Qlogic ISP PCI SCSI adapters should also work, however not necessarily for booting.

Graphics

All on-board graphics adapters are supported for text mode via STI routines (similar to PC VGA BIOS). At the present there is no working X server.

Human I/O

Human I/O is supported via PS/2 devices, HIL does not work.

Misc

Several PCI USB adapters from VIA and ALi have been tested and are known to work; they support USB mass-storage and Ethernet devices. The onboard Harmony audio system is supported.

3.4.4 Software

- ◇ NetBSD/hp700 4.0.1 release³⁹ <ftp.netbsd.org>

3.4.5 References

Manuals

- ◇ [INSTALL.html](#)⁴⁰ (ftp) installation instructions for NetBSD 4.0.1 release, NetBSD.org (October 2008, accessed January 2009)

Websites

- ◇ NetBSD/hp700⁴¹ official port page, NetBSD.org (n.d., accessed January 2009)

³⁹ <ftp://ftp.netbsd.org/pub/NetBSD/NetBSD-4.0.1/hp700/>

⁴⁰ <ftp://ftp.netbsd.org/pub/NetBSD/NetBSD-4.0.1/hp700/INSTALL.html>

⁴¹ <http://www.netbsd.org/Ports/hp700/>

3.5 NeXTSTEP/hppa

3.5.1 Overview

NeXTSTEP was introduced in 1989 as an UNIX implementation by NeXT. NeXTSTEP features a complete development and user environment, an unique GUI, a special display system, the DPS (Display Post Script). The underlying core is a Mach microkernel, 4.3BSD compatible and extensible at runtime. At the time of its introduction 1989, NeXTSTEP v0.8 only ran on the so called *black hardware*, rather expensive Motorola 68k systems also produced by NeXT. In 1991 Version 3.1 was introduced and for the first time *white hardware* (x86) was supported. The development line (68k and x86) was continued and around 1994 Version 3.3 with support for several RISC computers was released, including Sun SPARC and HP PA-RISC 1.1 systems.

The 715/100XC workstation is probably the fastest “non-white” (not Intel-based) workstation compatible with the original NeXTSTEP.

NeXTSTEP is a very interesting alternative on the older 32-bit workstations that support it. It generally feels much faster and more polished than contemporary HP-UX. However NeXTSTEP for PA-RISC lacks many current applications — the system shows its age.

Note that there are two important patches to apply to a vanilla NeXTSTEP 3.3, cf. the References for the descriptions and link.

3.5.2 Supported systems

NeXTSTEP runs on several 32-bit PA-RISC workstations with either PA-7100 or PA-7100LC processors and ASP or LASI chipset.

- ◇ 712
- ◇ 715
- ◇ 725
- ◇ 735
- ◇ 755

3.5.3 Supported hardware

- ◇ About 400MB of disk space for a common environment — complete developer environment around 700MB
- ◇ 32MB of RAM sufficient — 64MB better
- ◇ Maximum of 256MB RAM supported
- ◇ All onboard graphics and CRX and CRX-24 supported
- ◇ HCRX and HCRX-24 graphics supported after installation of the NeXTSTEP 3.3 patches
- ◇ On 712 and 715/{64,80,100} workstations only PS/2 keyboards supported, no HIL
- ◇ All other systems support HIL

- ✧ **Unsupported** on the 735/755 are the FWD (Fast/Wide Differential) SCSI subsystem and the optional FDDI network boards

3.5.4 References

Manuals

- ✧ **NeXTstep 3.3 Network and System Administration Manual**⁴² NeXT Software Inc. (1994). [Converted HTML version: Randall J. Rencsok (2000: channelu.com mirror)]
- ✧ **NeXTstep 3.3 Developer Documentation Manuals**⁴³ NeXT Software Inc. (1994). [Converted HTML version: Randall J. Rencsok (2000: channelu.com mirror)]

Other documents

- ✧ **The NEXTSTEP/OpenStep FAQ**⁴⁴ Bernhard Scholz (2000?). [Mirrored at channelu.com, original .org unavailable]

Software

- ✧ **NeXTSTEP Current Patch List**⁴⁵ (.pdf) Apple Computer, Inc (2006, mirrored at NeXTComputers.org. Accessed 8 January 2009)
- ✧ NeXTSTEP 3.3 “User” patch **NS33RISCUUserPatch3.tar**⁴⁶ (.tar) and its release notes **NeXTSTEP 3.3 Patch 3 Overview**⁴⁷ (.pdf) Apple Computer, Inc (2006, mirrored at NeXTComputers.org. Accessed 8 January 2009)
- ✧ NeXTSTEP 3.3 “Developer” patch **NS33DeveloperPatch2.tar**⁴⁸ (.tar)

There used to be a large software archive available at the Peanuts.org FTP server. It went offline about 2004-2005, apparently without a complete mirror of it anywhere.

⁴² <http://www.channelu.com/NeXT/NeXTStep/3.3/nsa/index.html>

⁴³ <http://www.channelu.com/NeXT/NeXTStep/3.3/nd/index.html>

⁴⁴ <http://www.channelu.com/NeXT/NeXTFAQ-new/NeXTFAQ.toc.html>

⁴⁵ http://www.nextcomputers.org/NeXTfiles/Software/NEXTSTEP/Patches/nextstep_current_patch_list.pdf

⁴⁶ http://www.nextcomputers.org/NeXTfiles/Software/NEXTSTEP/Patches/NEXTSTEP_3.3_User_Patch_3/NS33RISCUUserPatch3.tar

⁴⁷ http://www.nextcomputers.org/NeXTfiles/Software/NEXTSTEP/Patches/NEXTSTEP_3.3_User_Patch_3/nextstep3.3_patch_3_overview.pdf

⁴⁸ http://www.nextcomputers.org/NeXTfiles/Software/NEXTSTEP/Patches/NEXTSTEP_3.3_Developer_Patch_2/NS33DeveloperPatch2.tar

3.6 OpenBSD/hppa

3.6.1 Overview

The port of the **OpenBSD**⁴⁹ Unix-like operating system to HP PA-RISC computers (OpenBSD/hppa) focuses on 32-bit workstations and some 64-bit models running in 32-bit mode.

The current (as of Fall 2008) release of OpenBSD/hppa is **4.4** and has more or less full support for the listed systems and hardware.

Work on an OpenBSD port to PA-RISC HP 9000/700 systems was started by **Michael Shalayeff**⁵⁰ around 1999. Main sources of information and code at that time were mainly the previous porting efforts Lites/HPPA and MkLinux. The first more or less complete OpenBSD/hppa release was version 3.5, albeit still with limitations many unsupported machines and I/O devices.

NetBSD/hp700 is heavily based on OpenBSD/hppa, from the codebase of around 2001.

An **OpenBSD/hppa64** port to support PA-RISC 2.0 computers running in **64-bit** mode was started preliminary in 2007, but will probably not succeed due to lack of maintainership.

3.6.2 Supported systems

- ◇ 705, 710, 712, 715, 720, 730, 750, 725, 735, 755
- ◇ 742i 743i, 744, 745i, 745, 747i, 748i, 748
- ◇ A180[C]
- ◇ B132L, B160L, B132L+, B180L+, B1000, (*See Note 1*) B2000, B2600 (*See Note 1*)
- ◇ C100, C110, C132L, C160L, C160, C180 (*See Note 1*), C200, C240, C360, (*See Note 1*) C3000, C3600, C3650, C3700, C3750 (*See Note 1*)
- ◇ D220, D230, D320, D330
- ◇ J200, J210[XC], J2240, (*See Note 1*) J5000, J5600, (*See Note 1*) J6000, J6700, J6750, (*See Note 1*) J7000, J7600 (*See Note 1*)
- ◇ RDI PrecisionBook
- ◇ SAIC Galaxy 1100

Notes

1. System (hardware) is 64-bit but running in 32-bit mode

Unsupported systems: PA-RISC 1.0 systems and the older HP 9000/800 servers (Nova, the E-Class, and the even older systems). Also in doubt are some of the newer 64-bit server systems (with the **rp** designations), due to their very special chipsets and I/O systems.

⁴⁹ <http://www.openbsd.org>

⁵⁰ <http://mickey.lucifier.net>

3.6.3 Supported hardware

Processors

32-bit PA-RISC 1.0 PA-7000, PA-7100, PA-7100LC, PA-7200 and PA-7300LC; some systems with 64-bit processors in 32-bit mode: PA-8000, PA-8200, PA-8500, PA-8600 and PA-8700.

Buses and chipsets

All PCI, GSC and Runway buses and onboard bus controllers (ASP, LASI, Dino/Cujo, U2/Uturn, Astro and Elroy) on the above machines are supported. Additionally, Yenta-compatible PCI-Cardbus bridges are supported, as for instance found on the RDI Precisionbook.

ISA/EISA and HP-PB buses and bus controllers are not supported. Support for the EISA bus controller is in progress.

Networking

All on-board Ethernet and Fast-Ethernet network interfaces on the above machines are supported; the FDDI on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet (10, 100 and Gigabit) chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel EtherExpress PRO/10 and PRO/100 series, Intel Gigabit chipsets, in various incarnations for the PCI bus, NE2000-compatible, 3Com 3c9xx EtherLink XL) should also work. PCMCIA (and to a lesser extent Cardbus) devices are supported in a compatible PCI-Cardbus bridges, including various WLAN and Ethernet cards (the OpenBSD port page has the current and complete list).

Storage

Storage is at the moment supported via either the NCR 53C700 narrow, NCR 53C710 Fast-Narrow, NCR 53C720 Fast-Wide (HVD/differential) or the NCR 53C875 Ultra-Wide SE SCSI controllers. GSC/HSC and PCI expansion cards with one of the 53C7xx or 53C8xx SCSI chipsets and Adaptec 2940 PCI SCSI adapters should also work, though are not necessarily bootable.

Various newer PCI SCSI controllers based on Adaptec (AHA) and LSI Fusion-MPT chipsets are also supported, though also not bootable.

Graphics

All on-board graphics adapters are supported for text-mode via STI routines (similar to PC VGA BIOS), additionally the CRX, CRX-24, HCRX-8, HCRX-24, Visualize-EG and Visualize-FX (FX2, FX4 and FX6) graphics expansion boards (GSC and PCI) are supported. At the present, there is no working X server for OpenBSD/hppa, so there are no graphics (X11) capabilities for now.

Human I/O and multimedia

Input/output is supported via PS/2 or HIL on-board interfaces, though not all HIL devices are supported.

Various USB devices are supported, including networking adapters and I/O devices attached to expansion USB controllers (PCMCIA/PCI).

The on-board 16-bit “Harmony” audio device, found on many PA-RISC workstations, is supported.

3.6.4 Software

Releases

- ◇ OpenBSD/hppa 4.4 release⁵¹ [ftp.openbsd.org](ftp://ftp.openbsd.org)
- ◇ OpenBSD/hppa snapshots⁵² [ftp.openbsd.org](ftp://ftp.openbsd.org)

Add-on software

- ◇ Available through the OpenBSD packages system, both for **the current release**⁵³ (currently 4.4) and **the new snapshots**⁵⁴.
- ◇ Cf. **OpenBSD: Getting Packages**⁵⁵
- ◇ More software is available through the **OpenBSD Ports tree**⁵⁶, a framework for compiling open source software.

3.6.5 References

Manuals

- ◇ **INSTALL.hppa**⁵⁷ (snapshot) installation instructions, OpenBSD (January 2009: accessed January 2009)
- ◇ **INSTALL.hppa**⁵⁸ (4.4 release) installation instructions, OpenBSD (August 2008: accessed January 2009)

Websites

- ◇ **OpenBSD/hppa**⁵⁹ official page, The OpenBSD Project (August 2007. Accessed 27 August 2007)
- ◇ **OpenBSD/hppa64**⁶⁰ official page, The OpenBSD Project (May 2005. Accessed January 2009)

⁵¹ <ftp://ftp.openbsd.org/pub/OpenBSD/4.4/hppa/>

⁵² <ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/hppa/>

⁵³ <ftp://ftp.openbsd.org/pub/OpenBSD/4.4/packages/hppa/>

⁵⁴ <ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/packages/hppa/>

⁵⁵ <http://www.openbsd.org/ports.html#Get>

⁵⁶ <http://www.openbsd.org/ports.html#Use>

⁵⁷ <ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/hppa/INSTALL.hppa>

⁵⁸ <ftp://ftp.openbsd.org/pub/OpenBSD/4.4/hppa/INSTALL.hppa>

⁵⁹ <http://www.openbsd.org/hppa.html>

⁶⁰ <http://www.openbsd.org/hppa64.html>

Other documents

- ◇ Michael Shalayeff: **OpenBSD on PA-RISC talk**⁶¹ NYCBUG (2007: NYCBUG 2005 talk. Accessed January 2009)

⁶¹ <http://www.nycbug.org/index.php?NAV=Home;SUBM=83>

3.7 Research PA-RISC Operating Systems

(With input from Mike Hibler)

3.7.1 Overview

Several other operating systems have been ported to the PA-RISC platform over the time. Most of them only reached development state and have long been not maintained anymore. Documentation is rare and getting sources or distributions even more so.

These systems were based on four kernels/platforms:

1. **Mach (CMU) microkernel**

- ◇ Mach 3/UX, based on Mach 3 with AT&T System V Unix on top; from the University of Utah
- ◇ Mach 4/Lites, based on Mach 4 with a port of 4.4BSD-lites Unix on top; from the University of Utah
- ◇ MkLinux, based on Mach 3 with Mach 4 extensions with Linux 2.0 on top; from OSF RI
- ◇ HP Tut, based on Mach 2 with HP-UX 2.0 on top; from HP Labs

[Mach has been more or less abandoned since as a development/research project but was also used in the commercial NeXTSTEP 3.3 PA-RISC. For more information on Mach, cf. the **Mach (kernel) page from Wikipedia**⁶².]

2. **OSF Mach microkernel — OSF/1**

- ◇ HP OSF/1 based on Mach 2 with OSF/1 1.0 on top; from HP/ex-Apollo
- ◇ MK-PA (OSF/1), based on OSF Mach 3 with OSF/1 1.3 on top; from OSF RI

3. **BSD: HPBSD**, based on a modified 4.3BSD with 4.4BSD modifications; from the University of Utah

4. **Chorus** microkernel (INRIA), similar to Mach: Chorus, based on Chorus v3.3/v3.4 with System V Unix (MiX) on top; from Oregon Graduate Institute

Only MkLinux and Mach 4/Lites were publically available, the other systems all required proper licenses (which almost nobody had) for the various commercial sources contained in them. All of these ports were basically succeeded by the current open source systems—PA-RISC Linux, OpenBSD/hppa and, *maybe*, NetBSD/hp700.

Approximate timeline:

Table 3.1: PA-RISC R&D operating systems timeline

Year	HP	Utah	OSF	Other
1988	HP Tut			
1989	HP Tut	HPBSD		
1990	HP OSF/1	HPBSD		Chorus (835)
1991	HP OSF/1?	Mach 3/UX		Chorus (720)
1992				
1993		HPBSD 2.0		
1994		Mach 4/Lites	MK-PA 6.0	[NeXTSTEP 3.3]

⁶² http://en.wikipedia.org/wiki/Mach_kernel

1995			MK-PA 6.3	
1996		Mach 4/Lites II	MK-PA 7.x	
1997			MkLinux	

3.7.2 Mach 3/UX

Architecture: Mach 3/System V Unix

Released: 1991 (development)

One of the various Mach microkernel ports to PA-RISC (in this case Mach 3) was done in 1991 by Bob Wheeler of the University of Utah. This port should accomplish what the HP Tut project probably failed — a proper port of Mach to PA-RISC. The sole target system at the time was the HP 9000/835 server.

Ported were the Mach 3 microkernel, with a “proof-of-concept” AT&T-encumbered Unix (System V) kernel (“personality”) running as user-level server (the Unix part was originally done by CMU). The Mach 3/UX port never got very far, but code wound up later in the Mach 4/Lites port also done at Utah University and probably the Mach 3/OSF/1 (MK-PA) port from OSF.

It is unclear if there was a separate University of Utah OSF/1 to PA-RISC porting effort (Mach 3/OSF/1) — some sources suggest there was a short-lived project to port Mach 3.0 and OSF/1 1.0.4 to PA-RISC.

3.7.3 Mach 4/Lites

Architecture: Mach 4/4.4BSD-lite

Released: 1994 (original), 1996 (snapshot II)

The University of Utah Flux Research Group ported the original Mach microkernel (based on the work of the Mach 3/UX project) with a 4.4BSD-Lites server on it to the PA-RISC architecture, under the direction of Jay Lepreau. The operating system was developed in the early to mid-1990s and “released” from 1994-1996. There was never real support for and no enhancements made, thus it was quickly discontinued in favor of other projects (both at Utah University and elsewhere—for example the MkLinux port and others).

The project was seen from the beginning not as a complete operating system but rather as a snapshot for developers:

“We refer to this as a snapshot and not a release as the provided code is not robust, does not provide a complete application environment, contains minimal bootstrap capability, and has practically no documentation. Hence, we recommend that you do not run this, unless you are a hard-core O.S. hacker who has an interest in, and knowledge of, the PA architecture. Later true releases, with help from you O.S. hackers, will allow the more faint-at-heart to run an alternative O.S. on their HP workstations.”

Some parts of the PA-RISC source code of it were later actually useful in the ports of modern open source operating systems; OpenBSD/hppa used parts of the source code as reference and the later relicensed HP spmath floating point emulation library.

Supported Hardware

◇ 705, 710, 720, 730, 750 (based on PA-7000 processors)

- ◇ 715, 725, 735, 755 (based on PA-7100 processors)
- ◇ 712 [apparently last-minute changes to the snapshot prevent it from running/booting correctly on the otherwise supported 712s], 715 (based on PA-7100LC processors)
- ◇ Internal single-ended and fast-wide different SCSI drives and tapes, RS232 serial, builtin Ethernet, GRX and CRX graphics (Artist on 712/715 probably too), HIL and PS/2 keyboard/mouse
- ◇ *Unsupported*: FDDI networking, EISA expansion cards (and devices), parallel ports, audio, tele-share port (on 712) and floppy drives

Details

(Taken from the original Utah webpage, and modified, with permission from Mike Hibler⁶³)

Mach 4/Lites features support for the PA-RISC 1.1 (“HP 9000/700”) platform with the following components: freely distributable source, binaries, and boot image for a complete Mach kernel that includes some of Utah’s then-recent research (though not exploited), the Lites BSD-based single-server, include directories and libraries, and a complete GNU toolchain for the ELF object format. In addition, there are several other PA-RISC-related device drivers, kernel components and utilities. A fairly complete 4.4BSD-lite user environment is also provided. The entire system was self-built on Mach 4/Lites.

The operating system kernel is based on a **Mach** kernel, with the source derived from CMU’s (Carnegie Mellon University) MK83 release, and is loosely referred to as “Mach 4.” It contains some initial work done at Utah as part of the ARPA-funded *Fast and Flexible Mach Systems* work. In particular it contains a prototype implementation of migrating threads and a basic framework for signature-based RPC (remote procedure calls), a fundamental component of the presentation/interface work. None of these features is used either by the Lites server or within the kernel itself.

The PA-RISC specific portion includes all the necessary interrupt, exception, and system call handling code (“locore”), a pmap module, and device drivers for the VSC and GSC bus based workstations. The only kernel or server component provided only as a binary library and not in source form is the floating point emulation code which handles operations and exceptional conditions not done in hardware. The source is HP-proprietary, and the distributed `spmath` library could not be used for commercial purposes (later changed). The `libmach` and `libcthreads` libraries are also included with the necessary changes for PA-RISC support.

Also included is additional code never integrated into Mach 4. The code is either part of Utah’s earlier HP 9000/800 series PA-RISC 1.0 Mach 3/UX, HP 9000/700 OSF/1 ports (HP OSF/1 by HP) or Utah’s 4.3/4.4 hybrid BSD system (HPBSD). The former includes bus configuration and rudimentary device drivers for the CIO bus based workstations and servers as well as a remote kernel/task debugging facility developed by Convex. The latter includes some basic EISA support and alternative LAN drivers.

The Unix which runs on top of the Mach kernel is **Lites**: an 4.4BSD-lite (Berkeley Unix) operating system “personality” provided by the Lites server/emulator. Lites is a user-mode, single-task implementation of BSD Unix which runs on top of a Mach micro-kernel. It was developed by Johannes Helander at Helsinki University of Technology (HUT) in Finland.

References

- ◇ **The Utah PA-RISC Code Snapshot**⁶⁴ Original webpage of the project. Mike Hibler (January

⁶³ <http://www.flux.utah.edu/~mike/>

⁶⁴ <http://www.cs.utah.edu/flux/mach4-parisc/html/pamach.html>

1996 [correctly December 2002]: University of Utah. Accessed 21 March 2008)

- ◇ <ftp://flux.cs.utah.edu/flux/mach/ALPHA/>⁶⁵ (FTP) contains the snapshots sets for a complete systems, University of Utah (1994-2002. Accessed 21 March 2008)
- ◇ **Installation on HP 700s**⁶⁶ Utah PA-RISC Code Snapshot installation instructions. Mike Hibler (n. d.: University of Utah. Accessed 21 March 2008)
- ◇ **Frequently Asked Questions about the Utah PA-RISC Code Snapshot**⁶⁷ Mike Hibler (September 1995: University of Utah. Accessed 21 March 2008)

3.7.4 MkLinux

Architecture: Mach 3 with Mach 4 extensions/Linux

Released: 1997

MkLinux was a research project done in the mid to late-1990s by The Open Group/OSF to port a Linux kernel as server on top of a Mach microkernel (the Open Group's pmk1.1). The project built on the previous porting effort of OSF RI of the OSF/1 operating system to Mach on PA-RISC—the MK-PA (OSF Mach 3/OSF/1) project. OSF took various parts of the PA-RISC kernel sources from the Utah University, including the Mach 3/UX and Mach 4/Lites projects, improved the underlying OSF PA-RISC/Mach kernel (the Open Group RI Microkernel pmk1.1 from MK-PA) and put a Linux kernel (2.0.32) as server (“personality”) on it (replacing BSD/Lites). Included were X11R6 patches, the GNU ELF compiler and debugger and complete /usr and /var directories.

MkLinux was the first free operating system that truly *ran* on PA-RISC hardware (in contrast to Mach, which suffered from unfinished development and a lot of bugs on PA-RISC). However, the system was quite slow (with some blaming it on the underlying Mach microkernel), software support was rather crude and at the time of its active development PA-RISC workstations were not really largely distributed to private end-users. It also did not support shared libraries.

Supported Hardware

- ◇ 705, 710, 720, 730, 750 (based on PA-7000 processors)
- ◇ 715 (no /33), 725, 735, 755 (based on PA-7100 processors)
- ◇ 712, 715, 725/100 (based on PA-7100LC processors)
- ◇ C100, C110 (based on PA-7200 processors)
- ◇ SCSI (internal single-ended, internal fast-wide-differential, GSC-based fast-wide-differential, and EISA fast-differential), RS232 serial, builtin Ethernet, Video (GRX, CRX and Artist), HIL and PS/2, audio

References

- ◇ <ftp://ftp.cirr.com/pub/hppa/mklinux/>⁶⁸ (FTP) Mirror of the MkLinux sets at ftp.cirr.com

⁶⁵ <ftp://flux.cs.utah.edu/flux/mach/ALPHA/>

⁶⁶ <http://www.cs.utah.edu/flux/mach4-parisc/html/install-parisc.html>

⁶⁷ <http://www.cs.utah.edu/flux/mach4-parisc/html/pamach-faq.html>

⁶⁸ <ftp://ftp.cirr.com/pub/hppa/mklinux/>

- ◇ **Release Notes for MkLinux on HP PA-RISC**⁶⁹ (FTP) Descriptions on MkLinux and extensive installation instructions. The Open Group (1997 [Central Iowa (Model) Railroad mirror 1999]. Accessed 5 October 2005)

3.7.5 HP Tut

Architecture: HP Mach 2/HP-UX

Released: 1988/89 (development)

Tut was the name of project at HP Labs done at 1988-89 to get HP-UX running on a Mach microkernel. The project possibly never succeeded very far and switched to merging parts of Mach 2.0 (VM and tasks/threads?) into/under HP-UX 2.0 to get something close to resembling Mach on PA-RISC (1.0). It was the basis for various other porting efforts.

3.7.6 HP OSF/1

Architecture: HP Mach 2/OSF/1

Released: 1990 (development), 1991-1992 (product?)

Around 1990 an internal HP project started a port of an early version of the OSF/1 (OSF/1 1.0) operating system to PA-RISC. OSF/1 was the proposed Unix operating system by an alliance of DEC (Digital), IBM, HP and others to compete with AT&T's and Sun's System V Unix. The HP project was apparently independent of OSF's own later effort to port OSF/1 to PA-RISC (MK-PA, which started several years later).

HP OSF/1 was developed by ex-Apollo staff, after Apollo was bought by HP (at the times there were also rumours of OSF/1 for 68k-based HP/Apollo systems). They ported the Mach 2.0 ("macrokernel") to the early HP 9000/700 workstations (PA-RISC 1.1 based), resulting in a fairly complete operating system, with proper hardware support and a usable desktop environment (Motif and other OSF/1 applications). The port was however never widely distributed and only sold for a short time as a commercial product, which was withdrawn quickly (probably due to not complete/competitive hardware and software support when compared to internal and external competitors). It was however used widely at the University of Utah.

3.7.7 MK-PA (OSF/1)

Architecture: Mach 3/OSF/1

Released: 1994, 1995, 1996

The OSF RI (Open Group Research Institute) did a port of their OSF/1 Unix to PA-RISC—they ported OSF/1 1.3 onto Mach 3, with OSF/1 running as a server on top of the Mach microkernel. The results of the porting efforts were OSF MK6.0-PA (1994), MK6.3-PA (July 1995), MK7-PA (Jan 1996) and MK7.x-PA (March 1996).

Hardware support focused on the newer PA-RISC 1.1 700s workstations, support for the 800s PA-RISC 1.0 servers was dropped (from the original Mach 3/UX code base). MK-PA had as its main objectives: "establish the PA-RISC as an OSF RI reference platform, performance parity between HP-UX and

⁶⁹ <ftp://ftp.cirr.com/pub/hppa/mklinux/mkpa-rel.html>

MK based system, HP-UX binary compatibility, high-speed networking capability” (and others). Performance tests showed that for “low to moderate loads” the performance of MK-PA and HP-UX was similar while under heavy loads MK-PA achieved better results, probably due to VM enhancements. The MK-PA version 7.1 introduced real-time support to PA-RISC, including “Kernel preemption, Real-time clock” and an “Event Trace and Analysis Package (ETAP).” HP-UX compatibility was provided for HP-UX 9.05 on the MK-PA 7.1 release; compatibility for HP-UX 10 was apparently achieved with MK-PA 7.2.

The version of Mach 3 used by the OSF porting effort contained several of the “Mach 4” enhancements of the University of Utah (in-kernel servers and migrating threads) and probably used parts of the Mach 3/UX PA-RISC codebase. Parts of the MK-PA port were used as the base of the OSF’s port of Linux onto the OSF Mach microkernel — MkLinux.

Supported Hardware

- ◇ 710, 720, 730 (based on PA-7000 processors)
- ◇ 715, 725, 735, 755 (based on PA-7100 processors)
- ◇ 712, 715, 725/100 (based on PA-7100LC processors)
- ◇ J200, J210[XC], (based on PA-7200 processors)
- ◇ Additionally to standard hardware: Interphase FDDI board, EISA Ethernet boards, HP Labs GSC bus Myrinet board

References:

- ◇ **An HP-UX compatible microkernel based Operating System**⁷⁰ (FTP) The Open Group (1998 [Central Iowa (Model) Railroad mirror 2008]. Accessed 30 March 2008)
- ◇ **MK-PA Project Update**⁷¹ (FTP) James Loveluck (1996: The Open Group [Central Iowa (Model) Railroad mirror 2008]. Accessed 30 March 2008)

3.7.8 HPBSD

Architecture: 4.3/4.4BSD

Released: 1989 (original work), 1993 (HPBSD 2.0)

Mike Hibler’s HPBSD was the first non-commercial complete operating system for the PA-RISC platform. Developed at the University of Utah, it grew out of a port of 4.3BSD to the 68k-based HP 9000/300 and 400 systems. Since HPBSD contains AT&T (Unix) and HP (HP-UX) source code it was never freely available. Organizations with the necessary license agreements with HP and AT&T were able to obtain bootable releases but distribution outside of University of Utah was very limited. Active work mainly happened during the early and mid-1990s, with only small fixes committed afterward.

HPBSD is an “original” 4.3BSD with additions from 4.4BSD and local (Utah) modifications. Summarized:

- ◇ 4.4BSD C library and include files

⁷⁰ <ftp://ftp.cirr.com/pub/hppa/mklinux/.osf-website/os/hp-pa/index.htm>

⁷¹ <ftp://ftp.cirr.com/pub/hppa/mklinux/.osf-website/os/hp-pa/hp-slides/index.html>

- ◇ 4.4BSD filesystem code (includes Macklem/CSRG Berkely NFS; FFS; MFS)
- ◇ 4.4BSD networking code
- ◇ 4.3BSD filesystem layout
- ◇ 4.3BSD VM system

Supported Hardware

- ◇ 705, 710, 720, 730, 750 (based on PA-7000 processors)
- ◇ 715, 725, 735, 755 (based on PA-7100 processors)
- ◇ 712, 715, 725/100 (based on PA-7100LC processors)
- ◇ J200, J210[XC], C100, C110 (based on PA-7200 processors)
- ◇ *Early HPBSD*: HP 9000/835 server (PA1.0 NS-1 processor) — support dropped later on after the advent of PA-RISC 1.1 systems
- ◇ SCSI (internal single-ended, internal fast-wide-differential, GSC based fast-wide-differential, and EISA fast-differential) drives and DAT tapes, RS232 serial, builtin Ethernet, SGC FDDI board, Video (GRX, CRX and Artist), HIL and PS/2, audio

History

(Taken from the original HPBSD webpage, and modified, with permission from Mike Hibler⁷²)

HPBSD for 68k-based systems was born in 1987 when Mike Hibler started a port of 4.3BSD to the HP 9000/320 and 350 workstations at the University of Utah. Major development lasted until about 1991 with the final addition of Motorola 68040 support.

In the fall of 1989, Jeff Forys started work on a HP 9000/800 port based on the hybrid HP-UX/Mach kernel called Tut done as an experiment at HP Labs. By around February 1990 HPBSD was running on an 9000/835 and later that year was running solidly on the PA-RISC. For a short period of time in 1989-90, Mt Xinu also worked on the PA-RISC port and produced the first usable part of it, the boot loader, late in 1989. HPBSD used this boot loader. In 1990 another Mach project was spun off of HPBSD — the Mach 3/UX single server port for the 9000/835 sponsored by HP and primarily done by Bob Wheeler. Starting in May 1991, Leigh Stoller ported HPBSD to the HP 9000/720 workstation, after which support for PA-RISC 1.0 and the 9000/800 platform was dropped.

The last major development to HPBSD was the addition of the 4.4BSD kernel filesystem and networking code and the 4.4BSD ANSI-compliant C library. Jeff Forys started this in April 1992 and by early 1993 all of the University of Utah's HPBSD machines had been converted. This version was known as HPBSD 2.0. Since this merge included the NFS implementation done by Rick Macklem, all Sun encumbered code could be eliminated. In April 1993, a semi-formal release of HPBSD 2.0 was made to the 2-3 sites which had the necessary agreements with HP (necessary to obtain the PA-RISC specific code). Since that time, active development of HPBSD had pretty much stopped. As of Summer 1999, there were less than ten HPBSD machines left: one 68k and the rest PA-RISC. The last significant efforts were to bring HP-UX compatibility up to 10.20 (to run the JDK) and to port a 3Com EISA 100Mbit ethernet driver.

⁷² <http://www.flux.utah.edu/~mike/>

References

- ◇ **HPBSD: Utah's 4.3bsd port for HP9000 series machines**⁷³ Original homepage of the HPBSD project. Mike Hibler (July 1999: University of Utah. Accessed 4 October 2005)

3.7.9 Chorus

Architecture: Chorus/System V Unix (MiX)

Released: 1990 (development original project), 1991/92 (development follow-on)

Chorus was a micro-kernel (similar to Mach) based operating system, developed at **INRIA in France**⁷⁴ starting in 1979. A development effort was made to port Chorus to the PA-RISC architecture and hardware in 1990-1991 at the Oregon Graduate Institute (OGI).

The porting effort, a funded research project lead by **Jonathan Walpole**⁷⁵, was based on the Chorus v3.3 nucleus ("kernel") with the Chorus/MiX v3.2 on it and targeted the then recent HP 9000/834 "workstation" (PA-RISC 1.0 NS-1 processor). Hardware support was quite limited however, as apparently no network interfaces or disk devices were supported and all console I/O depended on PDC and IODC (PA-RISC "BIOS") routines. Code from various earlier projects were used, including source code from HP-UX 2.0 and the HP Tut project (HP-UX on 2.0 Mach). The port succeeded up to the stage that Unix shells and various system calls worked, but no access to file systems was possible.

A later porting project was started by Jon Inouye (also from Oregon Graduate Institute) to port the Chorus/MiX v3.2 with the newer v3.4 nucleus to the PA-RISC 1.1 9000/720 workstation (which was quite a popular target for OS/Unix porting efforts at that time). The port did not progress very far, as it supported very few device drivers; it was apparently used for "virtual memory experiments." In contrast to the earlier (9000/834) port it used HP-UX 8.0 as a base.

Both ports were never distributed as they contained various copyrighted/licensed source code (from HP, Chorus, USL, etc.).

Chorus/MiX in the version 3 was a complete System V Unix (both SVR32 and SVR4) compatible distributed operating system, however based on micro-kernel and with additional real-time and multi-threading features. The system is divided into the **nucleus** which is the underlying operating system core which "handles scheduling, memory management, real-time events, and communications." The nucleus is quite tiny ("typically only 50 to 60 KB in size") and the only truly platform-dependent part of the system. The rest of the operating system are implemented as **servers** (including device drivers, the Unix environment, Unix job and memory control, network support and sockets, etc.) that sit on top of the nucleus and communicate with each other and the kernel by passing messages. **MiX** is in this case a group of subsystems/servers that implement the aforementioned System V compatible Unix on top of the Chorus nucleus.

References

- ◇ **Porting Chorus to the PA-RISC: Project Overview**⁷⁶ (PDF, 0.1MB) Walpole, Jonathan, et al. OGI Technical Report No. CS/E-92-003 (January 1992: Oregon Graduate Institute)

⁷³ <http://www.cs.utah.edu/~mike/hpbsd/hpbsd.html>

⁷⁴ <http://www.inria.fr/index.en.html>

⁷⁵ <http://web.cecs.pdx.edu/~walpole>

⁷⁶ ftp://ftp.parisc-linux.org/docs/whitepapers/1992-chorus_reports/92-003.pdf

- ◇ **Porting Chorus to the PA-RISC: Overall Evaluation**⁷⁷ (PDF, 0.1MB) Walpole, Jonathan, et al. OGI Technical Report No. CS/E-92-003 (January 1992: Oregon Graduate Institute)
- ◇ **Modularity and Interfaces in Micro-Kernel Design and Implementation: A Case Study of CHORUS on the HP PA-RISC**⁷⁸ (PDF, 0.1MB) Walpole, Jonathan, et al. In Proceedings of the Usenix Workshop on Micro-Kernels and Other Kernel Architectures (Seattle, WA) April 1992
- ◇ **The Chorus Microkernel**⁷⁹ Pountain, Dick. BYTE magazine (January 1994)
- ◇ **Re: Chorus Ports - comp.os.chorus**⁸⁰ Jon Inouye (November 1994: USENET posting. Accessed March 2008)

⁷⁷ ftp://ftp.parisc-linux.org/docs/whitepapers/1992-chorus_reports/92-008.pdf

⁷⁸ ftp://ftp.parisc-linux.org/docs/whitepapers/1992-chorus_reports/CS-TR-92-49.pdf

⁷⁹ <http://www.byte.com/art/9401/sec8/art3.htm>

⁸⁰ <http://groups.google.com/group/comp.os.chorus/msg/157638c6c32b30ad?dmode=source>

Chapter 4

PA-RISC Computer Systems

4.1 PA-RISC Computers

4.1.1 Workstations

Portable/Laptop

Three portable PA-RISC computers were produced, all by third-party vendors: RDI/Tadpole, SAIC and Hitachi. The former two are based on the HP 712 and C132/C160L workstations' designs

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
RDI PrecisionBook 132	PA-7300LC 132MHz	128KB L1 (1MB L2)	512MB	2 Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 160	PA-7300LC 160MHz	128KB L1 (1MB L2)	512MB	2 Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 180	PA-7300LC 180MHz	128KB L1 (1MB L2)	512MB	2 Cardbus	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 60MHz	64KB	128MB	2 PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 80MHz	256KB	128MB	2 PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
Hitachi 3050RX/100C	Hitachi PA/50L	12KB	80MB		HI-UX/WE2 (Hitachi)

Pizzabox

Small, “pizza-box” sized integrated desktop computers.

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
705	PA-7000 35MHz	96KB	128MB	None	HP-UX, Linux, OpenBSD
710	PA-7000 50MHz	96KB	128MB	None	HP-UX, Linux, OpenBSD
712/60	PA-7100LC 60MHz	64KB	128MB	1 GIO 1 TSIO	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
712/80	PA-7100LC 80MHz	256KB	128MB	1 GIO 1 TSIO	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
712/100	PA-7100LC 100MHz	256KB	192MB	1 GIO 1 TSIO	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD

Desktop

PA-RISC computers in different desktop formats, from rather small (715, B-Class) to wide and heavy cases (730/735, C-Class).

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
715/33	PA-7100 33MHz	128KB	192MB	1 EISA/SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
715/50	PA-7100 50MHz	128KB	256MB	1 EISA/SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
715/64	PA-7100LC 64MHz	256KB	256MB	1 EISA/GSC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD

715/75	PA-7100 75MHz	512KB	256MB	1 EISA/SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
715/80	PA-7100LC 80MHz	256KB	256MB	1 EISA/GSC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
715/100	PA-7100LC 100MHz	256KB	256MB	1 EISA/GSC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
715/100XC	PA-7100LC 100MHz	1MB	256MB	1 EISA/GSC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
720	PA-7000 50MHz	384KB	272MB	1 EISA 1 SGC	HP-UX, Linux, OpenBSD
725/50	PA-7100 50MHz	128KB	256MB	3 EISA 1 EISA/SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
725/75	PA-7100 75MHz	512KB	256MB	3 EISA 1 EISA/SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
725/100	PA-7100LC 100MHz	256KB	256MB	1 EISA 3 EISA/GSC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
730	PA-7000 66MHz	384KB	272MB	1 EISA 1 SGC	HP-UX, Linux, OpenBSD
735/99	PA-7100 99MHz	512KB	400MB	1 EISA 1 SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
735/125	PA-7150 125MHz	512KB	400MB	1 EISA 1 SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
B132L	PA-7300LC 132MHz	128KB L1 (1MB L2)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX, Linux, NetBSD, OpenBSD
B132L+	PA-7300LC 132MHz	128KB L1 (1MB L2)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX, Linux, NetBSD, OpenBSD
B160L	PA-7300LC 160MHz	128KB L1 (1MB L2)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX, Linux, NetBSD, OpenBSD
B180L+	PA-7300LC 180MHz	128KB L1 (1MB L2)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX, Linux, NetBSD, OpenBSD
B2600	PA-8600 500MHz	1.5MB	4GB	4 PCI	HP-UX, Linux, OpenBSD
C100	PA-7200 100MHz	512KB	1GB	1 GSC 3 EISA/GSC	HP-UX, Linux, OpenBSD
C110	PA-7200 120MHz	512KB	1GB	1 GSC 3 EISA/GSC	HP-UX, Linux, OpenBSD
C132L	PA-7300LC 132MHz	128KB L1 (1MB L2)	2GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX, Linux, NetBSD, OpenBSD
C160L	PA-7300LC 160MHz	128KB L1 (1MB L2)	2GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX, Linux, NetBSD, OpenBSD
C160	PA-8000 160MHz	1MB	3GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD
C180	PA-8000 180MHz	2MB	3GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD
C200	PA-8200 200MHz	1.5MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX, Linux, OpenBSD
C240	PA-8200 236MHz	4MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX, Linux, OpenBSD
C360	PA-8500 367MHz	1.5MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX, Linux, OpenBSD

Mini-Tower

Some PA-RISC computers were delivered in a minitower case, similar in size to standard PCs. The newer workstations (“four digits”) feature black PC-like cases while the older J-Class systems are built into heavy, beige minitowers.

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
B1000	PA-8500 300MHz	1.5MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
B2000	PA-8500 400MHz	1.5MB	4GB	4 PCI	HP-UX, Linux, OpenBSD
C3000	PA-8500 400MHz	1.5MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
C3600	PA-8600 552MHz	1.5MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
C3650	PA-8700 625MHz	2.25MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
C3700	PA-8700 750MHz	2.25MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
C3750	PA-8700+ 875MHz	2.25MB	8GB	6 PCI	HP-UX, Linux, OpenBSD
C8000	2 PA-8800/ PA-8900 900MHz/ 1.0GHz/ 1.1GHz	3MB L1 32MB L2/ 64MB L2	32GB	3 PCI-X 3 PCI 1 AGP Pro 8x	HP-UX
J200	1-2 PA-7200 100MHz	512KB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD
J210	1-2 PA-7200 120MHz	512KB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD
J210XC	1-2 PA-7200 120MHz	2MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD
J280	PA-8000 180MHz	2MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD (likely)
J282	1-2 PA-8000 180MHz	2MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX, Linux, OpenBSD (likely)
J2240	1-2 PA-8200 236MHz	4MB	4GB	1 PCI 1 PCI/EISA 3 GSC/PCI	HP-UX, Linux, OpenBSD
J5000	1-2 PA-8500 440MHz	1.5MB	8GB	7 PCI	HP-UX, Linux, OpenBSD
J5600	1-2 PA-8600 552MHz	1.5MB	8GB	7 PCI	HP-UX, Linux, OpenBSD
J6000	1-2 PA-8600 552MHz	1.5MB	16GB	3 PCI	HP-UX, Linux, OpenBSD
J6700	1-2 PA-8700 750MHz	2.25MB	16GB	3 PCI	HP-UX, Linux, OpenBSD
J6750	1-2 PA-8700+ 875MHz	2.25MB	16GB	3 PCI	HP-UX, Linux, OpenBSD
J7000	1-4 PA-8500 440MHz	1.5MB	16GB	7 PCI	HP-UX, Linux, OpenBSD
J7600	1-4 PA-8600 552MHz	1.5MB	16GB	7 PCI	HP-UX, Linux, OpenBSD

4.1.2 Servers

Tower/Deskside

Rather large and heavy server systems, from smaller towers (D-Class/E-Class) to desktside systems (K-Class and the older HP 9000/800 lettered servers).

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
750	PA-7000 66MHz	512KB	768	4 EISA 2 SGC	HP-UX, Linux, OpenBSD
755/99	PA-7100 99MHz	512KB	768MB	4 EISA 2 SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
755/125	PA-7150 125MHz	512KB	768MB	4 EISA 2 SGC	HP-UX, Linux, NetBSD, NeXTSTEP, OpenBSD
D200	PA-7100LC 75MHz	256KB	512MB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D210	PA-7100LC 100MHz	256KB	512MB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D220	PA-7300LC 132MHz	128KB L1 (1MB L2)	1GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux, OpenBSD
D230	PA-7300LC 160MHz	128KB L1 (1MB L2)	1GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux, OpenBSD
D250	1-2 PA-7200 100MHz	512KB	1.5GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D260	2 PA-7200 120MHz	2MB	1.5GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D270	1-2 PA-8000 160MHz	1MB	3GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D280	1-2 PA-8000 180MHz	2MB	3GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
D300	PA-7100LC 75MHz	256KB	512MB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
D310	PA-7100LC 100MHz	256KB	512MB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
D320	PA-7300LC 132MHz	128KB L1 (1MB L2)	1GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux, OpenBSD
D330	PA-7300LC 160MHz	128KB L1 (1MB L2)	1GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux, OpenBSD
D350	1-2 PA-7200 100MHz	512KB	1.5GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
D360	2 PA-7200 120MHz	2MB	1.5GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
D370	1-2 PA-8000 160MHz	1MB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux

D380	1-2 PA-8000 180MHz	2MB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
D390	1-2 PA-8200 240MHz	4MB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX, Linux
E25	PA-7100LC 48MHz	64KB	512MB	2-4 HP-PB	HP-UX, Linux, NetBSD
E35	PA-7100LC 64MHz	256KB	512MB	2-4 HP-PB	HP-UX, Linux, NetBSD
E45	PA-7100LC 80MHz	256KB	512MB	2-4 HP-PB	HP-UX, Linux, NetBSD
E55	PA-7100LC 96MHz	1MB	512MB	2-4 HP-PB	HP-UX, Linux, NetBSD
F10	PA-7000 32MHz	96KB	768MB	2 HP-PB	HP-UX
F20	PA-7000 48MHz	128KB	768MB	2 HP-PB	HP-UX
F30	PA-7000 48MHz	512KB	768MB	2 HP-PB	HP-UX
G30	PA-7000 48MHz	512KB	768MB	4 HP-PB	HP-UX
G40	PA-7100 64MHz	512KB	768MB	4 HP-PB	HP-UX
G50	PA-7100 96MHz	512KB	768MB	4 HP-PB	HP-UX
G60	PA-7100 96MHz	2MB	768MB	4 HP-PB	HP-UX
G70	1-2 PA-7100 96MHz	4MB	768MB	4 HP-PB	HP-UX
H20	1 PA-7000 48MHz	128KB	768MB	8 HP-PB	HP-UX
H30	PA-7000 48MHz	512KB	768MB	8 HP-PB	HP-UX
H40	PA-7100 64MHz	512KB	768MB	8 HP-PB	HP-UX
H50	PA-7100 96MHz	512KB	768MB	8 HP-PB	HP-UX
H60	PA-7100 96MHz	2MB	768MB	8 HP-PB	HP-UX
H70	1-2 PA-7100 96MHz	4MB	768MB	8 HP-PB	HP-UX
I30	PA-7000 48MHz	512KB	768MB	12 HP-PB	HP-UX
I40	PA-7100 64MHz	512KB	768MB	12 HP-PB	HP-UX
I50	PA-7100 96MHz	512KB	768MB	12 HP-PB	HP-UX
I60	PA-7100 96MHz	2MB	768MB	12 HP-PB	HP-UX
I70	1-2 PA-7100 96MHz	4MB	768MB	12 HP-PB	HP-UX
K100	PA-7200 100MHz	512KB	512MB	1 HSC 4 HP-PB	HP-UX, Linux
K200	1-4 PA-7200 100MHz	512KB	4GB	1 HSC 4 HP-PB	HP-UX, Linux
K210	1-4 PA-7200 120MHz	512KB	4GB	1 HSC 4 HP-PB	HP-UX, Linux
K220	1-4 PA-7200 120MHz	2MB	4GB	1 HSC 4 HP-PB	HP-UX, Linux

K250	1-4 PA-8000 160MHz	2MB	4GB	1 HSC 4 HP-PB	HP-UX, Linux
K260	1-4 PA-8000 180MHz	2MB	4GB	1 HSC 4 HP-PB	HP-UX, Linux
K370	1-6 PA-8200 200MHz	4MB	4GB	3 HSC 4 HP-PB	HP-UX, Linux
K380	1-6 PA-8200 240MHz	4MB	4GB	3 HSC 4 HP-PB	HP-UX, Linux
K400	1-4 PA-7200 100MHz	512KB	2GB	1-5 HSC 8 HP-PB	HP-UX, Linux
K410	1-4 PA-7200 120MHz	512KB	2GB	1-5 HSC 8 HP-PB	HP-UX, Linux
K420	1-4 PA-7200 120MHz	2MB	8GB	1-5 HSC 8 HP-PB	HP-UX, Linux
K450	1-4 PA-8000 160MHz	2MB	8GB	1-5 HSC 8 HP-PB	HP-UX, Linux
K460	1-4 PA-8000 180MHz	2MB	8GB	1-5 HSC 8 HP-PB	HP-UX, Linux
K570	1-6 PA-8200 200MHz	4MB	8GB	9 HSC 4 HP-PB	HP-UX, Linux
K580	1-6 PA-8200 240MHz	4MB	8GB	9 HSC 4 HP-PB	HP-UX, Linux

Rack-mountable (19")

Servers specially built for 19" racks, from the rather flat A-Class and medium-sized *rp3400/rp4400* and L- and R-Class to large N-Class and *rp7400/rp8400*.

Model	Height	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
A180	2U	PA-7300LC 180MHz	128KB	2GB	2 GSC/PCI	HP-UX, Linux, NetBSD, OpenBSD
A180C	2U	PA-7300LC 180MHz	128KB L1 1MB L2	2GB	2 GSC/PCI	HP-UX, Linux, NetBSD, OpenBSD
A400 rp2400/rp2430	2U	1 (See Note 1) (up to 6X)	depends	2GB	2 PCI	HP-UX, Linux
A500 rp2450/rp2470	2U	1-2 (See Note 1) (up to 7X)	depends	8GB	4 PCI	HP-UX, Linux
rp3410	2U	PA-8800 800MHz	3MB L1 32MB L2	6GB	2 PCI-X	HP-UX, Linux
rp3440	2U	1-2 PA-8800/ PA-8900 800MHz/ 1.0GHz	3MB L1 32MB L2/ 64MB L2	32GB	4 PCI-X	HP-UX
rp4410	4U	1-2 PA-8800/ PA-8900 800MHz/ 1.0GHz	3MB L1 32MB L2/ 64MB L2	128GB	6 PCI-X	HP-UX
rp4440	4U	1, 2, 4 PA-8800/ PA-8900 800MHz/ 1.0GHz	3MB L1 32MB L2/ 64MB L2	128GB	6 PCI-X	HP-UX
L1000 rp5400	7U	1-2 (See Note 1) (up to 5X)	depends	8GB	5 PCI	HP-UX, Linux
L1500 rp5430	7U	1-2 (See Note 1) (up to 8X)	depends	8GB	6 PCI	HP-UX

L2000 rp5450	7U	1-4 (<i>See Note 1</i>) (up to 5X)	depends	16GB	10 PCI	HP-UX, Linux
L3000 rp5470	7U	1-4 (<i>See Note 1</i>) (up to 8X)	depends	16GB	10 PCI	HP-UX, Linux
N4000 rp7400	10U	1-8 (<i>See Note 1</i>) (up to 7X)	depends	32GB	12 PCI	HP-UX, Linux
N4000 rp7405	10U	2-8 (<i>See Note 1</i>) (6X and greater)	depends	64GB	14/16 PCI	HP-UX
N4000 rp7410	10U	2-8 (<i>See Note 1</i>) (6X and greater)	depends	64GB	14/16 PCI	HP-UX
rp7420	10U	1-8 PA-8800 900MHz/ 1.0GHz	3MB L1 32MB L2	64GB	14 PCI	HP-UX
rp7440	10U	1-8 PA-8900 1.2GHz	3MB L1 64MB L2	128GB	15 PCI-X	HP-UX
rp8400/rp8410	17U	2-16 (<i>See Note 1</i>)	depends	64GB	16 PCI	HP-UX
rp8420	17U	1-16 PA-8800/ PA-8900 900MHz- 1.1GHz	3MB L1 32MB L2/ 64MB L2	256GB	16 PCI-X	HP-UX
rp8440	17U	1-16 PA-8900 1.1GHz	3MB L1 64MB L2	256GB	16 PCI-X	HP-UX
R380	6U	1-2 PA-8000 180MHz	2MB	3GB	4 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux
R390	6U	1-2 PA-8200 240MHz	4MB	3GB	4 EISA 1 GSC 3 EISA/GSC	HP-UX, Linux

Notes

1. These systems were available in different CPU configurations, denoted by a two-number/letter suffix:

- ◆ -36: PA-8500 360MHz with 1.5MB on-chip I/D L1 cache each
- ◆ -44: PA-8500 440MHz with 1.5MB on-chip I/D L1 cache each
- ◆ -5X: PA-8600 550MHz with 1.5MB on-chip I/D L1 cache each
- ◆ -6X: PA-8700 650MHz with 2.25MB on-chip I/D L1 cache each
- ◆ -7X: PA-8700 750MHz with 2.25MB on-chip I/D L1 cache each
- ◆ -8X: PA-8700 875MHz with 2.25MB on-chip I/D L1 cache each
- ◆ -9X: PA-8800 (dual-core) 900MHz with 3MB on-chip L1 and 32MB off-chip L2 cache each
- ◆ PA-8900 (dual-core) 800MHz-1.1GHz with 3MB on-chip L1 and 64MB off-chip L2 is probably also possible (suffix and affected models unknown)
- ◆ Itanium 2/IA64 processors are probably also possible on some models

Not all CPUs are/were available on all models.

Mainframe

These very large enterprise-class systems were designed for HPC and large database processing needs. They offer a large range of expansion options, including a large set of CPUs and lots of RAM.

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
9000/890	1-4 PA-7100? 60MHz	?MB	2.0GB	14 HP-PB	HP-UX

T500	1-12 PA-7100 90MHz	2MB	3.75GB	14-112 HP-PB	HP-UX
T520	1-12 PA-7150 120MHz	2MB	3.75GB	14-112 HP-PB	HP-UX
T600	1-12 PA-8000 180MHz	2MB L1 8MB L2	3.75GB	2-24 HSC 14-168 HP-PB	HP-UX
V2200	4-16 PA-8200 200MHz	4MB	16GB	24 PCI	HP-UX
V2250	4-16 PA-8200 240MHz	4MB	16GB	24 PCI	HP-UX
V2500 Node	2-32 PA-8500 440MHz	1.5MB	32GB	28 PCI	HP-UX
V2500 Cluster	4-128 PA-8500 440MHz	1.5MB	128GB	56-112 PCI	HP-UX
V2600 Node	2-32 PA-8600 552MHz	1.5MB	32GB	28 PCI	HP-UX
V2600 Cluster	4-128 PA-8600 552MHz	1.5MB	128GB	56-112 PCI	HP-UX
Convex SPP1000/CD	2-16 PA-7100 100MHz	2MB	4GB	16 SBus	SPP-UX
Convex SPP1000/XA Hypernode	2-8 PA-7100 100MHz	2MB	2GB	8 SBus	SPP-UX
Convex SPP1000/XA Cluster	8-128 PA-7100 100MHz	2MB	32GB	16-64 SBus	SPP-UX
Convex SPP1200/CD	2-16 PA-7200 120MHz	512KB	4GB	16 SBus	SPP-UX
Convex SPP1200/XA Hypernode	2-8 PA-7200 120MHz	512KB	2GB	8 SBus	SPP-UX
Convex SPP1200/XA Cluster	8-128 PA-7200 120MHz	512KB	32GB	16-64 SBus	SPP-UX
Convex SPP1600/CD	2-16 PA-7200 120MHz	2MB	4GB	16 SBus	SPP-UX
Convex SPP1600/XA Hypernode	2-8 PA-7200 120MHz	2MB	2GB	8 SBus	SPP-UX
Convex SPP1600/XA Cluster	8-128 PA-7200 120MHz	2MB	32GB	16-64 SBus	SPP-UX
HP/Convex SPP2000 S-Class Single Node	4-16 PA-8000 180MHz	2MB	16GB	24 PCI	SPP-UX
HP/Convex SPP2000 X-Class Cluster	8-512 PA-8000 180MHz	2MB	512GB	48-768 PCI	SPP-UX
Superdome	2-128 PA-8600/ PA-8700/ PA-8700+ PA-8800 PA-8900	varies	1TB	PCI-X	HP-UX

4.1.3 VME boards

Integrated PA-RISC systems on VME boards, technically based on HP 9000/715 and B-Class workstations. Common used were medical, industrial and military data measurement and real time control.

Model	CPU	Cache per CPU	RAM max.	Expansion	Operating systems
742i/50	PA-7100 50MHz	128KB	64MB	None	HP-UX, Linux, OpenBSD
743i/64	PA-7100LC 64MHz	256KB	256MB	(2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
743i/100	PA-7100LC 100MHz	256KB	256MB	(2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
744/132L	PA-7300LC 132MHz	128KB	1GB	(2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
744/165L	PA-7300LC 165MHz	128KB L1 512KB L2	1GB	(2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
745i/50	PA-7100 50MHz	128KB	128MB	4 EISA	HP-UX, Linux, OpenBSD
745i/100	PA-7100 100MHz	512KB	256MB	4 EISA	HP-UX, Linux, OpenBSD
745/132L	PA-7300LC 132MHz	128KB	1GB	4 EISA or 4 PCI (2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
745/165L	PA-7300LC 165MHz	128KB L1 512KB L2	1GB	4 EISA or 4 PCI (2 GSC-M or 4 PMC)	HP-UX, Linux, OpenBSD
747i/50	PA-7100 50MHz	128KB	128MB	2 EISA 1 SGC 6 VME	HP-UX, Linux, OpenBSD
747i/100	PA-7100 100MHz	512KB	256MB	2 EISA 1 SGC 6 VME	HP-UX, Linux, OpenBSD
748i/64	PA-7100LC 64MHz	256KB	256MB	4 EISA or 4 PCI (2 GSC-M or 4 PMC) 6 VME	HP-UX, Linux, OpenBSD
748i/100	PA-7100LC 100MHz	256KB	256MB	4 EISA or 4 PCI (2 GSC-M or 4 PMC) 6 VME	HP-UX, Linux, OpenBSD
748i/132L	PA-7300LC 132MHz	128KB	1GB	4 EISA or 4 PCI (2 GSC-M or 4 PMC) 6 VME	HP-UX, Linux, OpenBSD
748i/165L	PA-7300LC 165MHz	128KB L1 512KB L2	1GB	4 EISA or 4 PCI (2 GSC-M or 4 PMC) 6 VME	HP-UX, Linux, OpenBSD

4.1.4 Early systems

The Early PA-RISC Systems page describes the various PA-RISC servers introduced from 1986, based on PA-RISC 1.0 architecture and using custom TTL and NMOS processors.

Model	CPU	Cache	RAM max.	Expansion	Operating systems
822	NS-2 25MHz	32KB	128MB	HP-PB	HP-UX
825	NS-1 25MHz	16KB	96/112MB	CIO	HP-UX
832	NS-2 30MHz	128KB	128MB	HP-PB	HP-UX

834 835 635	NS-1 30MHz	128KB	96/112MB	CIO	HP-UX, early HPBSD, Mach 3/UX, Chorus
840	TS-1 8MHz	128KB	96/112MB	CIO	HP-UX
842	PCX 32MHz	1MB	?MB	HP-PB	HP-UX
845	NS-2 27.5MHz	256KB	96/112MB	CIO	HP-UX
850	NS-1 27.5MHz	128KB	256MB	CIO	HP-UX
852	PCX 50MHz	1MB	?MB	HP-PB	HP-UX
855	NS-2 27.5MHz	256KB	256MB	CIO	HP-UX
860	NS-2 27.5MHz	1MB	256MB	CIO	HP-UX
865	PCX 50MHz	768KB	512MB	CIO	HP-UX
870	1-4 PCX 50MHz	1MB <i>per CPU</i>	1GB	CIO	HP-UX

A separate page exists for the HP 9000/500 FOCUS systems (520, 530 et al), the 32-bit predecessors of the PA-RISC systems and HP's first Unix workstations (and first HP 9000s), running a very early, arcane version of HP-UX.

4.1.5 Other vendors

A small circle of third-party vendors produced and sold PA-RISC computers, primarily in Japan. All of them were part of the PRO Precision RISC organization, founded by HP to promote its PA-RISC platform.

Hitachi

Hitachi had several lines of computers with PA-RISC processors, including Hitachi-designed workstations (3050RX) and servers (3500), which run Hitachi's HP-UX variant—HI-UX/WE2 (apparently compatible). Hitachi also sold various OEM systems from HP in Japan, rebranded as Hitachi 9000V.

Mitsubishi

Mitsubishi Electric of Japan sold rebranded HP 9000 workstations in the early 1990s as OEM under the name “MELCOM ME RISC series,” as part of the PRO. Apparently only three models were sold (the original HP 9000 “snakes” workstations):

- ✧ ME/R7200 and ME/S7200: HP 9000/720
- ✧ ME/R7300 and ME/S7300: HP 9000/730
- ✧ ME/R7500 and ME/S7500: HP 9000/750

Oki

Similar to Mitsubishi in the early 1990s, Oki Electric Industry sold various PA-RISC workstations and servers from HP rebranded as OEM systems. These were integrated the “OKITAC” brand and shipped from 1992 onward:

- ◇ OKITAC 9000/800 Series: HP 9000/800 Nova servers
- ◇ OKITAC 9000 A Series: HP 9000/A180C
- ◇ OKITAC 9000 B Series: HP Visualize B1000
- ◇ OKITAC 9000 C Series: HP Visualize C3000
- ◇ OKITAC 9000 D Series: HP 9000 D-Class
- ◇ OKITAC 9000 J Series: HP Visualize J5000
- ◇ OKITAC 9000 K Series: HP 9000 K-Class
- ◇ OKITAC 9000 R Series: HP 9000 R380 and R390

Stratus

Stratus built a line of high-availability PA-RISC based servers called *Continuum*. Different models were sold over the time, starting with PA-7100 based systems and peaking in PA-8600 models.

Different operating systems were/are available, but most of these computers are able to run HP-UX, besides Stratus’ own FTX and VOS.

4.1.6 Itanium systems

At about the same time HP introduced the final PA-8800/PA-8900 based PA-RISC systems, first workstations with HP/Intel’s Itanium architecture were released by HP, shortly followed by Itanium servers. The Itanium/IA64 architecture (a *VLIW* architecture, called “EPIC” by HP in the 1980s/1990s) was originally designated the direct successor of PA-RISC (“PA-9000”) to be introduced in the mid-to-late 1990s.

Workstations

HP only produced three Itanium *workstations* before dropping Unix workstations completely, making these Itanium workstations the last (and probably fastest) HP-UX workstations.

Model	CPU (<i>See Note 1</i>) Itanium	Cache	RAM max.	Expansion	Operating systems
i2000	ME 733MHz/ 1-2 ME 800MHz	<i>varies</i>	16GB	7 PCI 1 AGP Pro 110	HP-UX, Linux, FreeBSD, Windows
zx2000	MK/MD/DF 900MHz-1.5GHz	<i>varies</i>	8GB	5 PCI-X 1 AGP Pro 4x	HP-UX, Linux, FreeBSD, Windows, (Open-VMS)
zx6000	1-2 MK/MD 900MHz-1.5GHz	<i>varies</i>	24GB	3 PCI-X 1 AGP Pro 4x	HP-UX, Linux, FreeBSD, Windows, (Open-VMS)

Notes

1. The specific Itanium processor types are noted by the two-letter abbreviations: Itanium first generation:

◇ ME: Merced

Itanium 2:

◇ MK: McKinley

◇ MD: Madison

◇ DF: Deerfield *low-voltage*

Servers

HP also released a line of Itanium-based servers, the rack-mountable *Integrity rx* line. (Missing entries for rxs will be added soon.)

Model	Height	CPU (See Note 1) Itanium	Cache	RAM max.	Expansion	Operating systems
rx1600 rx1600-2	1U	1-2 DF 1.0GHz	<i>varies</i>	16GB	2 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx1620	1U	1-2 FW 1.3-1.6GHz	<i>varies</i>	16GB	4 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2600 rx2600-2	2U	1-2 DF/MD 1.0-1.5GHz	<i>varies</i>	24GB	4 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2620	2U	1-2 MD/MC-D 1.3-1.6GHz	<i>varies</i>	32GB	4 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2660	2U	1-2 MV/MV-D 1.4-1.6GHz	<i>varies</i>	32GB	4 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx3600	4U	1-2 MV-D 1.4-1.6GHz	<i>varies</i>	96GB	8 PCI-X or / 4 PCI-X/4 PCIe	HP-UX, Linux, Windows, OpenVMS
rx4610	7U	2-4 ME 733-800MHz	<i>varies</i>	64GB	10 PCI	HP-UX, Linux, Windows
rx4640 rx4640-8	4U	1-4 MD/HD/MV 1.1-1.6GHz	<i>varies</i>	64GB	6 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx5670 rx5670-4	7U	1-4 MD 1.3-1.5GHz	<i>varies</i>	96GB	9(10) PCI-X	HP-UX, Linux, Windows, OpenVMS
rx6600	7U	1-4 MV-D 1.4-1.6GHz	<i>varies</i>	192GB	8 PCI-X or / 4 PCI-X/4 PCIe	HP-UX, Linux, Windows, OpenVMS
rx7620 rx7620-16	10U	2-8 MD/HD 1.1-1.5GHz	<i>varies</i>	64GB	15 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx7640 rx7640-16	10U	2-8 MC/MC-D/MV-D 1.4-1.6GHz	<i>varies</i>	256GB	15 PCI-X/ PCIe x8	HP-UX, Linux, Windows, OpenVMS
rx8620 rx8620-32	17U	2-16 HD/MD 1.1-1.6GHz	<i>varies</i>	256GB	16 PCI-X	HP-UX, Linux, Windows, OpenVMS
rx8640 rx8640-32	17U	2-16 MV-D 1.4-1.6GHz	<i>varies</i>	512GB	16 PCI-X or / 8 PCI-X/8 PCIe	HP-UX, Linux, Windows, OpenVMS
rx9610	rack	4-16 ME 733-800MHz	<i>varies</i>	128GB	64-128 PCI-X	HP-UX

Notes

1. The specific Itanium processor types are noted by the two-letter abbreviations:

Itanium first generation:

◇ ME: Merced

Itanium 2:

◇ MD: Madison

◇ FW: Fanwood *low-voltage*

◇ DF: Deerfield *low-voltage*

- ◇ MC: Montecito
- ◇ MC-D: Montecito *Dual-Core*
- ◇ MV: Montvale
- ◇ MV-D: Montvale *Dual-Core*
- ◇ HD: Hondo *Dual-CPU*

4.2 Early PA-RISC Systems

Information on these very early models and their details is sometimes quite incoherent. This includes HP documentation (both sales and technical), which not always describe the processor and system features of these computers coherently. In some cases, the system type was deduced—from supplied system block diagrams together with MIPS “benchmarks.” Computers names and model numbers were also compiled from various sources and may be not completely correct. (See Note 1)

4.2.1 840: First PA-RISC Server, TS-1 (TTL) (See Note 2)

The first commercial PA-RISC product appeared in 1986 with the **HP 9000/840** (*Indigo*) computer, based on a six-board TTL implementation of the 32-bit PA-RISC 1.0 architecture, TS-1, running at 8MHz. The TTL boards measure 8.4×11.3”, SRAMs/PALs and about 150 ICs each. The TS-1 boards implement the processor pipeline, a 4096-entry TLB and 128 KB (L1) cache, divided into 64 KB for each data and instruction.

Two main buses are used in the I/O system:

1. **Central Bus** (CTB—also called **MidBus**) connects the processor to the main memory and the secondary I/O bus (see below). CTB is 32-bit wide and has a clock speed of 8MHz, with a sustained transfer rate of 20MB/s. Seven slots for general purpose I/O cards are available.
2. **Channel I/O** (CIO) is the central device I/O bus. Up to three CIO buses (also called CIBs) are supported in a single 9000/840 computer. (Others mention only one CIO channel on the 9000/840—all three channels apparently were reserved for the very similar HP 3000/930.) CIO/CIB is 16-bit wide and achieves a transfer rate of 5MB/s with a clock speed of 4MHz. Seven (shared) I/O slots are available. Supported devices on CIO include HP-IB (*Hewlett-Packard Interface-Bus*, commonly used for instrumentation and measurement devices) and networking adapters.

Seven shared slots for I/O and memory are available, for up to 112MB of RAM (7×16MB; 2-16MB memory modules were supported). The optional graphics adapter used one I/O and one memory slot, reducing the maximum RAM to 96MB. Included by default into the system is a separate *Floating Point Coprocessor* (FPC) board. The 840 could be upgraded via a CPU board swap to 825, 835 or 845s retaining the case and memory and I/O boards.

It achieved about 4.5 MIPS and ran HP-UX version 1.0 (heavily BSD-based) up until version 10.01 (the pre-Y2k release). Storage and media devices were attached to the HP-IB bus, SCSI was only later (and with newer boot ROMs) available.

4.2.2 825, 835 and 850: NS-1 (NMOS)

One year later, 1987, first systems with 32-bit PA-RISC 1.0 processors implemented in NMOS-III logic, the PA-RISC NS-1, appeared: (See Note 3)

HP 9000/825 *FireFox* (also HP 9000/825S):

- ◇ 25MHz NS-1 processor on two boards
- ◇ 16KB cache
- ◇ 2048-entry TLB
- ◇ CTBs run at 8.33MHz

- ✧ Maximum RAM of 112MB (7×16MB), 96MB (6×16MB) with graphics adapter
- ✧ Seven shared I/O (CIO) and memory slots
- ✧ Performance of about 9 MIPS
- ✧ Price of about US \$42,500 at time of introduction
- ✧ Also sold with graphics hardware (825CHX included 2D adapter, 825SRX up to 24-bit 3D graphics)

HP 9000/835 *TopGun* (also HP 9000/835S):

- ✧ 30MHz NS-1 processor (Not completely clear if the 835 is really based on a NS-1 — performance figures (MIPS) and clock speed (all NS-2 have a maximum of 27.5MHz while the 835 has a CPU speed of 30MHz) point to a NS-1 while system diagrams point to a NS-2)
- ✧ 128KB cache
- ✧ 4096-entry TLB
- ✧ CTBs run at 10MHz (their maximum)
- ✧ Maximum RAM of 112MB (7×16MB), 96MB (6×16MB) with graphics adapter
- ✧ Seven shared I/O (CIO) and memory slots
- ✧ Performance of about 14 MIPS
- ✧ Price of about US \$45,000 at time of introduction
- ✧ Also sold with graphics hardware (835CHX included 2D adapter, 835SRX up to 24-bit 3D graphics)
- ✧ The 9000/834 was the same as a standard 835 however with a two-user limit
- ✧ The 9000/835SE is a high-end version with integrated CIO expander
- ✧ Server version (without graphics) shortly sold as 9000/635SV
- ✧ A port of early PA-RISC HPBSD ran on 834 and 835, as did an (unreleased) Mach 3.0 port (not the Mach 4/Lites for 700s workstations) from the University of Utah
- ✧ A in-progress port of the Chorus operating system (v3.3 nucleus — kernel — and v3.2 MiX — the operating system personality on top) was ported in 1990-1991 to the 834

HP 9000/850 *Cheetah* (also HP 9000/850S):

- ✧ 27.5MHz NS-1 processor
- ✧ 128KB cache (combined I/D)
- ✧ 4096-entry TLB
- ✧ CTBs run at 9.16MHz
- ✧ CIO I/O bus
- ✧ Maximum RAM of 128MB with one memory controller (MCo) and 256MB with two memory controllers (MCo, MC1) [it could be the 256MB/two MCs were only supported on the HP 3000 equivalents]
- ✧ Performance of about 14 MIPS

- ◇ Price of about US \$200,000 at time of introduction

RAM could be expanded with 16MB memory arrays, *i.e.*, memory boards.

The systems use three main buses, expanding the original 9000/840 architecture: (*See Note 4*)

- ◇ The 64-bit wide System Main Bus (SMB) connects the CPU, main memory and I/O (over CTBs) with a throughput of 100MB/s.
- ◇ Two CTBs/Midbuses (see **Central Bus** in the TS-1/TTL section) attach via two bus converters to the SMB
- ◇ In turn, the rest of the I/O devices are attached via CIO/CIBs (see **Channel I/O** above) to the two CTBs.
- ◇ The 850 additionally features two **Memory Array Buses** (MABs — MAB-0 and MAB-1), capable of linking up eight 16MB memory modules (arrays) via a 72-bit datapath the the SMB.

Earlier versions of this page listed four models as having a NS-1 CPU; however after careful review the 845 was moved to the NS-2 group of servers.

4.2.3 845, 855 and 860: NS-2 (NMOS)

Later, in 1989, similar computers based on the NS-2, a revamped NS-1, appeared (from early 1989 till late 1990). The later PA-RISC 1.0 and CIO bus based servers include: (*See Note 5*)

HP 9000/845 *ShoGun*:

- ◇ 27.5MHz NS-2 processor (not completely clear if this system is in fact based on a NS-1 or NS-2 — performance figures (MIPS) and cache/TLB sizes point to the latter)
- ◇ 256KB cache
- ◇ 16384-entry TLB
- ◇ CTBs run at 9.16MHz
- ◇ Maximum RAM of 112MB (7×16MB), 96MB (6×16MB) with graphics adapter
- ◇ Seven shared I/O (CIO) and memory slots
- ◇ Performance of about 22 MIPS
- ◇ Server version (without graphics) shortly sold as 9000/645SV

HP 9000/855 *Jaguar* (also HP 9000/855S):

- ◇ 27.5MHz NS-2 processor
- ◇ 256KB cache (separate I/D)
- ◇ 16384-entry TLB
- ◇ CTBs run at 9.16MHz
- ◇ Maximum RAM of 128MB with one memory controller (MCo) and 256MB with two memory controllers (MCo, MC1) [it could be that 256MB/two MCs were only supported on the HP 3000 equivalents]
- ◇ Performance of about 22 MIPS
- ◇ Price of about US \$300,000 at time of introduction

HP 9000/860 (also HP 9000/860S) *Cougar*:

- ✧ 27.5MHz NS-2 processor
- ✧ 1024KB cache (separate I/D)
- ✧ 16384-entry TLB
- ✧ CTBs run at 9.16MHz
- ✧ Maximum RAM of 128MB with one memory controller (MCo) and 256MB with two memory controllers (MCo, MC1) [it could be the 256MB/two MCs were only supported on the HP 3000 equivalents]

These systems are all based on the same I/O architecture and CIO devices and facilitate the same CPU design — PA-RISC 1.0 NS-2. The 860 could be upgraded with newer CPU boards to a 865 or 870 (see below).

4.2.4 865 and 870: PCX (CMOS)

The 9000/865 and the multi-processor 9000/870 (the first PA-RISC SMP system) include the first PA-RISC processors implemented in CMOS — the PA-RISC 1.0 PCX. These systems are very similar to the NS-2 based servers (with the 860 being board-upgradeable to a 865 or 870) and feature the same principal system and I/O architecture (with a slightly modified CPU/SPU architecture). (*See Note 6*) These system use the same 16MB memory arrays as earlier servers but could additionally use 64MB boards.

HP 9000/865 *Panther*:

- ✧ 50MHz PCX processor
- ✧ 768KB cache (separate I/D)
- ✧ 8192-entry TLB
- ✧ CIO bus for I/O
- ✧ Maximum RAM of 512MB

HP 9000/870 *Panther* (also HP 9000/870S):

- ✧ First (SMP) multiprocessor PA-RISC system
- ✧ Up to four 50MHz PCX processors
- ✧ 870/100 was uni-processor, 870/200 dual, 870/300 tri and 870/400 quad
- ✧ 1024KB cache (separate I/D)
- ✧ 8192-entry TLB
- ✧ CIO bus for I/O
- ✧ Performance of about 50 MIPS (single-CPU), 90 MIPS (dual-CPU)
- ✧ Maximum RAM of 1024MB with two memory controllers (MCo, MC1) in 16 slots (16×64MB) [it could be the 1024MB were only supported on the HP 3000 equivalents]
- ✧ Price of about US \$440,000 for 870/300, \$530,000 for 870/400

4.2.5 822, 832, 842 and 852: Low-Cost NS-2 and PCX

Shortly after, in 1989, lower-end and more compact servers were introduced, apparently also based on the NS-2 and PCX processors but already using the HP-PB I/O bus: (*See Note 7*)

HP 9000/822 *SilverFox Low*:

- ◇ 25MHz NS-2 processor
- ◇ 32KB cache (separate I/D)
- ◇ 4096-entry TLB
- ◇ Maximum RAM of 128MB (some sources say 64MB)
- ◇ Performance of about 10 MIPS
- ◇ Price of about US \$20,000 at time of introduction

HP 9000/832 *SilverFox High*:

- ◇ 30MHz NS-2 processor
- ◇ 128KB cache (separate I/D)
- ◇ 4096-entry TLB
- ◇ Maximum RAM of 128MB (some sources say 64MB)
- ◇ Performance of about 15 MIPS
- ◇ Price of about US \$30,000 at time of introduction

HP 9000/842 *SilverBullet Low*:

- ◇ 32MHz PCX processor
- ◇ 1024KB cache (separate I/D)
- ◇ 8192-entry TLB
- ◇ Performance of about 30 MIPS

HP 9000/852 *SilverBullet High*:

- ◇ 50MHz PCX processor
- ◇ 1024KB cache (separate I/D)
- ◇ 8192-entry TLB
- ◇ Performance of about 50 MIPS

These 8x2 servers were described as all having CMOS PCX processors in previous versions of this page. This is apparently not correct, as the 822/832 HP brochures state that these systems had NMOS CPUs, with the system block diagrams pointing to a NS-2. The picture for these systems is not really clear, with available benchmark results pointing in an even different direction.

4.2.6 Benchmarks

Assorted MIPS “benchmark” numbers for systems with known, unambiguous results, in ascending order.

Model	MIPS
840	4.5
825	9
822	10
850	14
835	14
832	15
845	22
855	22
842	30
852	50
870/100single	50
870/200 dual	90

4.2.7 References

1. **INFORMATION ON HP9000 SERVERS AND WORKSTATIONS**¹ Hewlett Packard Company (1999. Accessed January 2007) and **The HP 3000/HP 9000 model spreadsheet**² (Excel spreadsheet) Allegro Consultants (2004. Accessed January 2007)
2. Wayne E. Holt (ed.), *Beyond RISC! An Essential Guide to Hewlett-Packard Precision Architecture*, p. 95-102. (January 1988: Software Research Northwest Inc.) and **Hardware Design of the First HP Precision Architecture Computers**³ (PDF) David A. Fotland et al (March 1987: Hewlett-Packard Journal)
3. **HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook**⁴ (PDF) Hewlett-Packard Company (October 1990. Accessed January 2008 at hpmuseum.net) and **HP 9000 Series 800 Model 825S Hardware Technical Data**⁵ (PDF) Hewlett-Packard Company (September 1988. Accessed January 2008 at hpmuseum.net) and **HP 3000/925 and HP 9000/825/835 Computer Systems CE Handbook**⁶ (PDF) Hewlett-Packard Company (May 1988. Accessed January 2008 at hpmuseum.net) and **New midrange members of the Hewlett-Packard Precision Architecture Computer Family**⁷ Thomas O. Meyer et al (June 1989: Hewlett Packard Journal. Accessed January 2008 at findarticles.com)
4. Wayne E. Holt, *Beyond RISC!*
5. Hewlett-Packard Company, *HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook*
6. Ibid.
7. **HP 9000 Series 800 Model 822S/832S Technical Data**⁸ (PDF) Hewlett-Packard Company (1989. Accessed January 2008 at hpmuseum.net)
8. For HP 9000/840: Interview with David Fotland, September/October 2008

¹ http://www.parisc-linux.org/documentation/hp9000_models.html

² http://www.allegro.com/papers/HPPA_Systems.xls

³ <http://hpmuseum.net/document.php?catfile=372>

⁴ <http://www.hpmuseum.net/document.php?hwfile=4049>

⁵ <http://www.hpmuseum.net/document.php?hwfile=3343>

⁶ <http://www.hpmuseum.net/document.php?hwfile=4048>

⁷ http://findarticles.com/p/articles/mi_moHPJ/is_n3_v40/ai_7397316

⁸ <http://www.hpmuseum.net/document.php?hwfile=2652>

4.3 HP 9000/705 & 710

4.3.1 Overview

The HP 9000/705 and HP 9000/710 are miniaturized versions of the original PA-RISC “Snakes” (720, 730 and 750). The internals of these basically were taken over, with some significant changes:

- ◇ Smaller I/D caches
- ◇ Lower CPU clock rate
- ◇ Different (narrower) connection to the memory subsystem
- ◇ Integration of several subsystems (graphics, SCSI, Ethernet) onto a single mainboard
- ◇ Reduced expansion possibilities

Introduced: 1992 for \$7,490 (HP 9000/710)

4.3.2 Internals

CPU

- ◇ 705: PA-7000 35MHz with 32/64KB off-chip I/D L1 cache
- ◇ 710: PA-7000 50MHz with 32/64KB off-chip I/D L1 cache

Chipset

- ◇ ASP chipset
 - NCR 53C700 8-bit single-ended SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - WD16C552 parallel
 - NS16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC
 - * system & user timers
 - * HP-HIL interface
 - * frontpanel system status LEDs
- ◇ Viper memory and I/O controller, low-cost version implemented in two chips
- ◇ Intel 82C501AD Ethernet transceiver
- ◇ PSB2160 CODEC for 8-bit mono audio

Buses

- ◇ PBus processor/memory bus, 200MB/s at 50MHz (710), 140MB/s at 35MHz (705)
- ◇ VSC main system bus, 100MB/s at 25MHz (710), 70MB/s at 17.5MHz (705)
- ◇ GSC system-level I/O bus
- ◇ SCSI-2 narrow single-ended bus

Memory

- ◇ HP-proprietary 72-pin SIMMs
- ◇ Eight sockets
- ◇ 16MB (4×4) minimum, 64MB maximum
- ◇ Memory has to be installed in *quartets*:
first in the “even” slots (0, 2, 4, 6), then in the “odd” slots (1, 3, 5, 7):

```

              front
. ~~~~~ .
| ext.      int.      ###|
| drive     drive     ###|
|           ###|
|           ###|
|           ###|
| 3 x-----x 7 x-----x ###<--Power
| 2 x-----x 6 x-----x ###| Supply
| 1 x-----x 5 x-----x ###|
| 0 x-----x 4 x-----x ###|
. ~~~~~ .
              back

```

Expansion

- ◇ No expansion slots

Drives

- ◇ One tray for a 3.5" 50-pin Narrow SE SCSI hard drive
- ◇ One tray for a half-height 5.25" 50-pin Narrow SE SCSI drive, external accessible

4.3.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel

- ◇ 15-pin AUI 10Mbit & 10Base2 BNC Ethernet
- ◇ HD15 VGA
- ◇ HP-HIL connector for input devices
- ◇ Two phone jacks (microphone, headphones)

4.3.4 References:

Articles

- ◇ **High-Performance Design for Low-Cost PA-RISC Desktops**⁹ (.pdf) pp. 56-63 Craig Fink et al (August 1992: Hewlett-Packard Journal)

4.3.5 Operating systems

- ◇ HP-UX: every release from 10.01-10.20 works.
 - 10.20: runs ok on them, but you should get the maximum of RAM.
 - 11.00: also could work, but a) it is unsupported, b) it is very slow and c) some HP-UX patches can leave the system in an unrunnable state.
- ◇ Linux: works.
- ◇ OpenBSD: works.

4.3.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
705	21.9	33.0		
710	31.6	47.6	0.99	1.44

⁹ <http://www.hpl.hp.com/hpjjournal/pdfs/IssuePDFs/1992-08.pdf>

4.4 HP 9000/712

4.4.1 Overview

The design goal of the 712 workstation was to reach performance levels of 1992-era workstations and servers (for instance HP 9000 735 workstation) at a fraction of their fabrication costs. Everything was kept simple, the case is one of the smallest Unix workstation cases, similar to the Sun SPARCstation 10 and 20 cases. 712s are very quiet, the fan of the power supply being almost not audible — the produced noise depends on the installed SCSI drive.

Introduced: early-1994 to mid-1995 (712/100)
prices from \$4,000 (712/60) and \$8,820 (712/80) to \$15,100 (712/100).

4.4.2 Internals

CPU

- ◇ 712/60: PA-7100LC 60MHz with 1KB on-chip L1 (*See Note 1*) and 64KB off-chip L1 cache
- ◇ 712/80: PA-7100LC 80MHz with 1KB on-chip L1 (*See Note 1*) and 256KB off-chip L1 cache
- ◇ 712/100: PA-7100LC 100MHz with 1KB on-chip L1 (*See Note 1*) and 256KB off-chip L1 cache

Notes

1. The 1KB on-chip L1 cache is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Artist graphics, 8-bit
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ Two AM29F010 Flash EPROMs

Buses

- ◇ GSC system level I/O bus (128MB/s)
- ◇ SCSI-2 single-ended bus

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32MB modules
- ◇ Either 4 (on /60 and /80 models) or 6 (on /100) sockets
- ◇ 16MB (2×8) minimum, 128MB (4×32)/ 192MB (6×32) maximum
- ◇ Memory has to be installed in pairs, starting from slot 0, which is the closest slot to the drives.

Expansion

- ◇ VRAM expansion slot for:
 - A2263-66520M - Video RAM expansion for higher resolutions/more colors
- ◇ One slot for a GIO card (special formfactor GSC bus cards, only used in the 712), with the following cards available:
 - A2878A - second video
 - A4011A - 8025 Token Ring interface
 - A4011B - 8025 Token Ring interface
 - A4013A - second serial port
 - A4014A - second Ethernet LAN (AUI+TP) and serial port.
 - A4015A - second serial & X25 link (DB9M RS232C connectors)
 - A4217A - second Ethernet LAN (AUI+TP) & second VGA
 - TAMS 50488 - HP-IB interface
- ◇ One slot for a TSIO card (another special formfactor GSC card for the *Teleshare* expansion slot), with only one card offered:
 - A4012A - Teleshare POTS interface with two RJ11C jacks

Drives

- ◇ One tray for a 3.5" Fast-Narrow SE 50-pin SCSI hard drive
- ◇ One tray for a 3.5" Floppy drive with special connector

4.4.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ DB9 male RS232C serial (up to 115200 baud)
- ◇ DB25 female parallel
- ◇ TP/RJ45 10Mbit Ethernet (*See Note 1*)
- ◇ 15-pin AUI 10Mbit Ethernet (*See Note 1*)
- ◇ HD15 VGA (*See Note 2*)
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Three phone jacks (microphone, headphones and line-in)

Notes

1. The system automatically detects the used port.
2. You can connect almost any monitor to the VGA jack. The 712 can drive VESA compatible multisync, HP fixed-frequency and many other popular FF monitors. It also is able to produce sync on green signals.

4.4.4 ROM update

There is an firmware update available for the 712, which contains the latest version (2.3).

- ◇ PF_C7120023.txt¹⁰ has details about the contents and installation of the patch.
- ◇ PF_C7120023¹¹ contains the patch.

4.4.5 References

Manuals

- ◇ Model 712 Technical Reference¹² (PDF, 3.7MB)
- ◇ Model 712 Service Handbook¹³ (PDF, 4.4MB)

Articles

- ◇ HP 9000 Model 712 Overview¹⁴ (PDF, HP Journal 4/95)
- ◇ Design of the Model 712's I/O subsystem (LASI)¹⁵ (PDF, HP Journal 4/95)
- ◇ Product design of the Model 712¹⁶ (PDF, HP Journal 4/95)

¹⁰ http://ftp.parisc-linux.org/kernels/712/PF_C7120023.txt

¹¹ http://ftp.parisc-linux.org/kernels/712/PF_C7120023

¹² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37629/lpv37629.pdf>

¹³ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37944/lpv37944.pdf>

¹⁴ <http://www.hpl.hp.com/hpjournal/95apr/apr95a1.pdf>

¹⁵ <http://www.hpl.hp.com/hpjournal/95apr/apr95a4.pdf>

¹⁶ <http://www.hpl.hp.com/hpjournal/95apr/apr95a9.pdf>

- ◇ In addition to the above almost the whole **HP Journal April 1995 Issue**¹⁷ deals with the 712 workstation.

Other

- ◇ **NetBSD 712 serial console HOWTO**¹⁸, instructions to configure 712s to use serial console (*i.e.*, run headless)
- ◇ Pinout for the AUI/RS232 Y-cable for the optional second Ethernet/serial card.

4.4.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.01-11.11 works.
 - 10.20: runs very nice on all 712s.
 - 11.00 and 11i: 712s are not the best 11.x performers. Could be sluggish.
- ◇ NeXTSTEP: version 3.3 works fine.
- ◇ Linux: works fine.
- ◇ OpenBSD: works fine.
- ◇ NetBSD: experimental support as of 5/2005.

4.4.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
712/60	67.0	85.3	2.08	2.66	18.7	23.9
712/80	97.1	123.3	3.12	3.55	28.1	32.0
712/100	117.2	144.2	3.76	4.06	33.8	36.3

4.4.8 Physical dimensions/Power

- ◇ 70×423×400 mm height/width/depth
- ◇ 8.36kg net weight
- ◇ 110W max. power input
- ◇ 1.2A max. RMS at 240V
- ◇ 2.7A max. RMS at 120V

¹⁷ <http://www.hpl.hp.com/hpjournal/95apr/apr95.htm>

¹⁸ http://www.netbsd.org/Ports/hp700/serialconsole-hp-9000_712.html

4.5 HP 9000/715

4.5.1 Overview

The HP 9000/715 range of computers are divided in two different series:

- ◇ The 715/33, 715/50 and 715/75 were the first 715 series, with PA-7100 processors and an older chipset/mainbus combination, ASP.
- ◇ The 715/64, 715/80, 715/100 and 715/100 are younger and technically identical to the 712 workstations.

They were introduced between 1992 (first models) and 1994-1995 (second generation). Introduction and prices:

Table 4.15: HP 9000/715 workstations, Introduction dates and Prices

Model	Introduced	Price (USD)
715/33	1992	\$4,995
715/50	1992	\$11,895
715/64	1994	\$10,000
715/80	1994	\$13,000
715/100	1994	\$19,000
715/100XC	1995	\$21,000

4.5.2 Internals

CPU

- ◇ 715/33: PA-7100 33MHz with 64/64KB off-chip L1 I/D cache
- ◇ 715/50: PA-7100 50MHz with 64/64KB off-chip L1 I/D cache
- ◇ 715/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 715/75: PA-7100 75MHz with 256/256KB off-chip L1 I/D cache
- ◇ 715/80: PA-7100LC 80MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 715/100: PA-7100LC 100MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 715/100XC : PA-7100LC 100MHz with 1KB on-chip I L1 and 1024KB off-chip unified I/D L1 cache

The 1KB on-chip L1 cache is not really a true cache.

Chipset

715/64, 715/80 and 715/100

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel

- Harmony CD/DAT quality 16-bit stereo audio
- NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP-HIL
- ◇ Artist graphics, 8-bit
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ Two AM29F010 Flash EPROMs

715/33, 715/50 and 715/75

- ◇ ASP chipset, featuring:
 - NCR 53C700 8-bit single-ended SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - WD 16C552 parallel
 - NS 16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC
 - * system & user timers
 - * audio generator
 - * HP-HIL interface
 - * frontpanel system status LEDs
- ◇ Viper memory and I/O controller
- ◇ Intel 82501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ CRX graphics, 8-bit
- ◇ CS4215 CODEC for 16-bit stereo audio

Buses

- ◇ GSC system level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 single-ended narrow bus
- ◇ 715/33, 715/50, 715/75: PBus processor/memory bus
- ◇ 715/33, 715/50, 715/75: VSC main system bus
- ◇ 715/33, 715/50, 715/75: SGC expansion of the mainbus to the SGC expansion card

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32MB modules
- ◇ Eight memory sockets
- ◇ 715/33: 6 memory sockets
- ◇ 16MB (2×8) minimum, 192MB (6×32) or 256MB (8×32) maximum

Expansion

- ◇ 715/33, 715/50, 715/75: One SGC (*EISA formfactor*) expansion slot
- ◇ 715/64, 715/80, 715/100: One GSC (*EISA formfactor*) expansion slot
- ◇ With an adapter card EISA cards can be used in the GSC or SGC slots

Drives

- ◇ Two trays for one 3.5" Fast-Narrow SE 50-pin SCSI hard drive each
- ◇ One tray for one half-height 5.25" Fast-Narrow SE 50-pin SCSI drive, externally accessible

4.5.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended Fast-Narrow
- ◇ Two DB9 male RS232C serial (up to 115200 baud)
- ◇ DB25 female parallel
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ HD15 VGA
- ◇ 715/33, 715/50, 715/75: HP-HIL connector for input devices
- ◇ 715/64, 715/80, 715/100: SMD-10 connector, to connect HIL/PS2 with a special adapter
- ◇ Four phone jacks (microphone, headphones and line-in and ?)

4.5.4 ROM update

There is a firmware update available for the 715/64, 715/80 and 715/100. *This however does not work on a 715/100XC.*

- ◇ C7X50016.text¹⁹ has details about the contents and installation of the patch.
- ◇ C7X50016.frm²⁰ contains the new firmware.

4.5.5 References

Manuals

- ◇ Model 715 Service Handbook²¹ (PDF, 5.1MB)

4.5.6 Operating systems

- ◇ 715/33, 715/50, 715/75: HP-UX: every release from 10.01-10.20 works.
 - 10.20: runs nice on them.
 - 11.00: also works, but is unsupported and slow (esp. on 715/33). Some HP-UX patches can leave the system in an unrunnable state.
- ◇ 715/64, 715/80, 715/100: HP-UX: every 32-bit release from 10.01-11.11 works.
 - 10.20: runs very nice these 715s.
 - 11.00 and 11i: you should get the maximum of RAM. Runs OK, though 10.20 probably is faster.
- ◇ NeXTSTEP: Version 3.3 works fine.
- ◇ Linux: works.
- ◇ OpenBSD: works fine.
- ◇ NetBSD: experimental support as of 5/2005.

4.5.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
715/33	32.5	52.4	1.01	1.58
715/50	49.2	78.8	1.53	2.46
715/64	80.6	109.4	2.52	3.31
715/75	82.6	127.2	2.51	3.85
715/80	96.3	123.2	3.01	3.50
715/100	115.1	138.7	3.76	4.06
715/100XC	132.2	184.6	4.55	4.70

¹⁹ <http://ftp.parisc-linux.org/kernels/715/C7X50016.text>

²⁰ <http://ftp.parisc-linux.org/kernels/715/C7X50016.frm>

²¹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37699/lpv37699.pdf>

4.6 HP 9000/720, 730 & 750

4.6.1 Overview

Project name:

These machines were the first PA-RISC workstations, called the *Snakes*, and were based on the first PA-RISC 1.1 processors. They were built into very solid cases, consisting of interlocking exchangeable modules (“sliders”). The storage subsystem has its own “slider” , connected to the main I/O board with a short external cable. The 720 and 730 share the same backplane and I/O board and can be upgraded through the exchange of the CPU board. Later HP 9000/735 workstations share a similar system setup and 720/730 CPU and I/O boards can be swapped *together* for 735 boards, and vice versa (as 735 I/O boards do not work with 720 CPU boards, both boards have to be exchanged).

Introduced: June 1991

prices between \$11,990 and \$118,190.

4.6.2 Internals

CPU

- ◇ 720: PA-7000 50MHz with 128/256KB off-chip I/D L1 cache
- ◇ 730: PA-7000 66MHz with 128/256KB off-chip I/D L1 cache
- ◇ 750: PA-7000 66MHz with 256/256KB off-chip I/D L1 cache

Chipset

- ◇ ASP chipset, featuring:
 - NCR 53C700 8-bit single-ended SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - WD 16C552 parallel
 - NS 16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC
 - * system & user timers
 - * HP-HIL interface
 - * frontpanel system status LEDs
- ◇ Viper memory and I/O controller
- ◇ Intel 82C501AD Ethernet transceiver

- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)

Buses

- ◇ PBus processor/memory bus at processor clock (720: 50MHz with 200MB/s, 730/750: 66MHz with 264MB/s)
- ◇ VSC main system bus at 0.5 of processor clock (720: 25MHz with 100MB/s, 730/750: 33MHz with 132MB/s)
- ◇ GSC system-level I/O bus
- ◇ EISA additional I/O expansion bus
- ◇ SGC expansion of the mainbus to the SGC expansion cards
- ◇ SCSI-2 narrow single-ended bus

Memory

- ◇ HP proprietary memory modules (some shared with 735/755)
- ◇ 720: 8 slots
- ◇ 730: 8 slots and 16MB onboard
272MB (8×32+16) maximum
- ◇ 750: 12 slots
768MB (12×64) maximum

Expansion

- ◇ 720/730:
 - one SGC (*DIO-II formfactor*) expansion slot
 - one EISA slot
- ◇ 750:
 - Two SGC (*DIO-II formfactor*) expansion slots
 - Four EISA slots

Drives

- ◇ 720/730: one tray for two 3.5" Narrow SE 50-pin SCSI hard drives
- ◇ 750: one tray for two half-height 5.25" Narrow SE 50-pin SCSI drives and two trays for one full-height 5.25" Narrow SE 50-pin SCSI drive each

4.6.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ Two DB9 male RS232C serial (up to 115200 baud)
- ◇ DB25 female parallel
- ◇ 15-pin AUI 10Mbit & 10Base2 BNC Ethernet
- ◇ Graphics depend on installed SGC framebuffer
- ◇ HP-HIL connector for input devices
- ◇ Jack for beep audio

4.6.4 References:

Manuals

- ◇ Model 720/730 owner's guide²² (PDF, 1.8MB)
- ◇ Model 750 owner's guide²³ (PDF, 2.1MB)

Articles

- ◇ Midrange PA-RISC Workstations with Price/Performance Leadership²⁴ (.pdf) pp. 6-11 Andrew J. DeBaets and Kathleen M. Wheeler (August 1992: Hewlett-Packard Journal)

4.6.5 Operating systems

- ◇ HP-UX: every release from 10.01-10.20 works.
 - 10.20: runs ok on them.
 - 11.00: also could work, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- ◇ Linux: works.
- ◇ OpenBSD: works since XXX.
[On a sidenote, the port to the 720 workstation took nine years to complete (since late 1999).]

4.6.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
720	36.4	58.2	1.20	2.00
730	47.8	75.4	1.50	2.30
750	48.1	75.0	1.50	2.30

²² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37630/lpv37630.pdf>

²³ http://ftp.parisc-linux.org/docs/platforms/750_owners-guide.pdf

²⁴ <http://www.hpl.hp.com/hpjournal/pdfs/IssuePDFs/1992-08.pdf>

4.7 HP 9000/725

4.7.1 Overview

These were designated to be smaller replacements for the old 750 servers while still offering the same amount of I/O options. They are technically based on their 715 workstations counterparts.

Introduced: 1992 (725/50) to 1994 for
\$17,895 (725/50).

4.7.2 Internals

CPU

- ◇ 725/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- ◇ 725/75: PA-7100 75MHz with 256/256KB off-chip I/D L1 cache
- ◇ 725/100: PA-7100LC 100MHz with with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

725/50 and 725/75

- ◇ ASP chipset.
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10Mb Ethernet controller
- ◇ WD 16C552 parallel
- ◇ NS 16550A compatible serial
- ◇ 512KB EPROM - the Boot ROM
- ◇ 8KB EEPROM for storing system configuration status etc.
- ◇ Intel 8042 microprocessor
- ◇ Intel 82501AD Ethernet transceiver
- ◇ CRX graphics, 8-bit
- ◇ CS4215 CODEC for 16-bit stereo audio
- ◇ Viper memory and I/O controller
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)

725/100

- ◇ LASI chipset.
- ◇ NCR 53C710 8-bit single-ended SCSI-2
- ◇ Intel 82596CA 10Mb Ethernet controller
- ◇ WD 16C522 compatible parallel
- ◇ Harmony CD/DAT quality 16-bit stereo audio
- ◇ NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP-HIL
- ◇ Artist graphics, 8-bit
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ Two AM29F010 Flash EPROMs

Buses

- ◇ GSC system-level I/O bus
- ◇ EISA additional I/O expansion bus
- ◇ 725/50, 725/75: PBus processor/memory bus
- ◇ 725/50, 725/75: VSC main system bus
- ◇ 725/50, 725/75: SGC expansion of the mainbus to the SGC expansion card
- ◇ SCSI-2 single-ended narrow bus (Fast on 725/100)

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32MB modules
- ◇ Eight sockets
- ◇ 32MB (2×16) minimum, 256MB (8×32) maximum

Expansion

- ◇ 725/50, 725/75: Three EISA expansion-slots,
One slot for either a SGC (*EISA formfactor*) or EISA card.
- ◇ 725/100: One EISA expansion slot,
Three slots for either GSC (*EISA formfactor*) or EISA cards.

Drives

- ◇ One tray for one 3.5" Narrow SE 50-pin SCSI hard drive
- ◇ One tray for one 3.5" Floppy drive
- ◇ Two trays for one half-height 5.25" Narrow SE 50-pin SCSI drive each, externally accessible
(725/100 supports Fast-Narrow drives)

4.7.3 External connectors

- ◇ 50-pin HD SCSI-2 Narrow SE single-ended (Narrow-fast on 712/100)
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ HD15 VGA
- ◇ 725/50, 725/75: HP-HIL connector for input devices
- ◇ 725/100: SMD-10 connector, to connect HIL/PS2 with a special adapter [pic]
- ◇ Four phone jacks (microphone, headphones, line-in and ?)

4.7.4 References

4.7.5 Operating systems

- ◇ 725/50, 725/75: HP-UX: every release from 10.01-10.20 works.
 - 10.20: runs nice on them.
 - 11.00: also works, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- ◇ 725/100: HP-UX: every 32-bit release from 10.01-11.11 works.
 - 10.20: runs very nice.
 - 11.00 and 11i: you should get the maximum of RAM. 10.20 is probably faster though.
- ◇ NeXTSTEP: Version 3.3 works fine.
- ◇ Linux: works.
- ◇ OpenBSD: works

◊ NetBSD: experimental support as of 5/2005.

4.7.6 Benchmarks

Model	SPEC95, int	SPEC95, fp
725/50	1.53	2.46
725/75	2.51	3.85
725/100	3.76	4.06

4.8 HP 9000/735 & 755

4.8.1 Overview

Project names:

The 735 and 755 are early-1990s technical and graphical workstations and computing servers. Both 735 (desktop) and 755 (tower) have a very solid and heavy casing and are built with several circuit boards, separate for I/O and CPU. These boards, along with EISA cages and the storage subsystem are built into so-called “sliders” that can be removed separately from the system. They support a large set of I/O buses, expansion options and drives. The 735 was widely used as a FDDI node in Convex clusters and one of the fastest RISC workstations running NeXTSTEP.

The 735 is built into a similar case to the HP 9000/720 workstations, and the CPU and I/O boards can be swapped between them (however only together).

Introduced: 1992 for

prices starting at \$37,395 (735/99) and \$58,995 (755/99).

4.8.2 Internals

CPU

- ✧ PA-7100 99MHz with 256/256KB off-chip I/D cache
- ✧ PA-7150 125MHz with 256/256KB off-chip I/D cache

Chipset

- ✧ ASP2 chipset, featuring:
 - *Cutoff* ASIC, interfacing with memory (*Viper*) and I/O buses, provides address decoding, bus arbitration and interrupts
 - *Shortstop* ASIC, coordinates data communication between the I/O buses and the mainbus
 - NCR 53C700 8-bit single-ended SCSI-2
 - NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - AMD Formac Plus Am79C830 FDDI controller
 - WD16C552 parallel, plus additional functionality provided through Cutoff, *e.g.*, Scanjet support
 - NS16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC

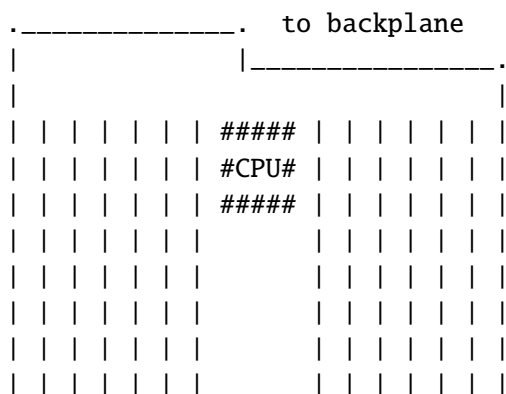
- * system & user timers
- * audio generator
- * HP-HIL interface
- * frontpanel system status LEDs
- ◇ Viper memory and I/O controller
- ◇ Intel 82C501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ CS4215 CODEC for 16-bit stereo audio

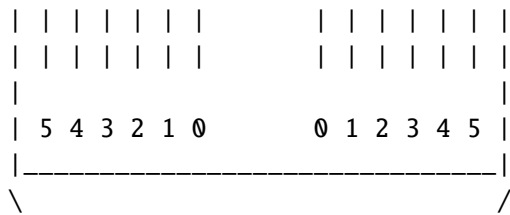
Buses

- ◇ PBus processor/memory bus, 66MHz on 735/99 and 755/99 (264MB/s)
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus
- ◇ EISA additional I/O expansion bus
- ◇ SGC expansion of the mainbus to the SGC expansion cards
- ◇ SCSI-2 narrow single-ended bus
- ◇ SCSI-2 Fast-Wide *high-voltage differential* (HVD) main storage I/O bus

Memory

- ◇ HP proprietary memory modules (same as 720, 730 and 750, and the Nova servers)
- ◇ 735: 8-32MB modules (most 64MB are unsupported and/or would not fit mechanically)
- ◇ 755: 8-64MB modules
- ◇ 12 sockets
- ◇ 735: 16MB onboard, 400MB (12×32+16) maximum
- ◇ 755: 768MB (12×64) maximum
- ◇ Memory has to be installed in pairs, from bank 0 to the outside on both sides equally:





Expansion

◇ 735:

- One SGC (*DIO-II formfactor*) expansion slot
- One EISA slot
- One special daughter card slot for:
 - * A2665A - FDDI SAS daughter card with MIC connector
 - * A2658A - AUI Ethernet daughter card
 - * A2831A - ThinLAN Ethernet daughter card

◇ 755:

- Two SGC (*DIO-II formfactor*) expansion slots
- Four EISA slots

Drives

- ◇ 735: one tray for either two 3.5" SCSI 68-pin Fast-Wide HVD or 50-pin narrow SE hard drives. Installed tray varies from model to model, 735/99 more often had the SE tray whereas the /125 models commonly had the F/W HVD tray.
- ◇ 755: one tray for two half-height 5.25" SCSI drives and two trays for one full-height 5.25" SCSI drive each

4.8.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended external
- ◇ 68-pin HD SCSI-3 Fast-Wide *high-voltage differential* HVD external
- ◇ Two standard RS232C serial
- ◇ DB25 parallel
- ◇ 735: 15-pin AUI or 10Base2 BNC Ethernet or FDDI SAS MIC connector
- ◇ 755: 15-pin AUI & 10Base2 BNC Ethernet connectors
- ◇ RGB BNC, depends on installed framebuffer, if at all
- ◇ HP-HIL connector for input devices
- ◇ Five phone jacks (microphone, headphones, line-in, line-out and speaker) (*optional on 755*)

4.8.4 References

Manuals

- ◇ Model 735 Service Handbook²⁵ (PDF, 7.6MB)

4.8.5 Operating systems

- ◇ HP-UX: every release from 10.01-10.20 works.
 - 10.20: works fine.
 - 11.00: the March 2000 release should be the last one that runs on these machines. Newer install CDs may even do not start at all. General Patch Releases from a date later than 03/2000 could make the installation unusable. HP-UX 11.00 is officially unsupported on these machines however.
 - 11i: officially unsupported on these systems, depending on the date of the installation CDs it might be possible to install it. It seems the system is stable once installed, however OS patches have to be carefully reviewed as some SCSI patches could render the system unusable.
- ◇ NeXTSTEP: Version 3.3 works fine, but the 53C720 Fast-Wide HVD SCSI subsystem and the FDDI boards are unsupported.
- ◇ Linux: works.
- ◇ OpenBSD: works fine.
- ◇ NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI controller is not supported.

4.8.6 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
/99	3.22	4.06	29.4	35.8
/125	3.97	4.61	36.3	40.9

²⁵ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38563/lpv38563.pdf>

4.9 HP 9000/742i VME Workstation

4.9.1 Overview

The *Sidewinder* is a so-called *Single Board Computer* (SBC), based on VME. It features basically the same core electronics as the 715/50 on a single board, but has fewer expansion possibilities—it takes only a small amount of RAM, has no on-board expansion slots and graphics hardware (serial console has to be used). The SCSI I/O is routed through the VME-P2 connector at the rear. Since the board features a VME controller it is able to talk to other VME devices on the same bus (and control them).

4.9.2 Internals

CPU

- ◇ PA-7100 50MHz with 64/64KB off-chip I/D L1 cache

Chipset

- ◇ ASP chipset, featuring:
 - NCR 53C700 8-bit single-ended SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - WD 16C552 parallel
 - NS 16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC
 - * system & user timers
 - * audio generator
 - * HP-HIL interface
 - * frontpanel system status LEDs
- ◇ Viper memory and I/O controller
- ◇ Intel 82501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ CRX graphics, 8-bit
- ◇ CS4215 CODEC for 16-bit stereo audio
- ◇ VME bus adapter

Buses

- ◇ PBus processor/memory bus
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus
- ◇ VME bus
- ◇ SCSI-2 narrow single-ended bus.

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32MB modules
- ◇ Two slots
- ◇ 16MB (2×8) minimum, 64MB (2×32) maximum

Expansion

- ◇ None

4.9.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ DB15 15-pin AUI 10Mbit Ethernet

4.9.4 References

Manuals

- ◇ 742i Owner's Guide²⁶ (PDF, 1.5MB)

4.9.5 Operating systems

- ◇ HP-UX: every 32-bit release from 9.01 to 10.20 works.
- ◇ Linux: should run.

4.9.6 Benchmarks

²⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00299/lpv00299.pdf>

Model	SPEC95, int	SPEC95, fp
742i/50	1.53	2.46

4.9.7 Physical dimensions/Power

- ◇ 40×233×160mm height/width/depth
- ◇ height of 2 VMEbus slots
- ◇ 0.91kg weight
- ◇ 35W @ +5V DC
- ◇ 0.12W @ +12V DC
- ◇ 0.12W @ -12V DC

4.10 HP 9000/743i & 744 VME Workstation

4.10.1 Overview

The *Anole* 743i and 744 workstations are VME *Single Board Computers* (SBCs). The whole system processing unit (SPU) together with the memory and several I/O controllers sit on a single-height 2U VME board, which needs to be installed in a fitting VME cage. This cage provides power and an VME bus connection for routing of I/O to either other VME boards (VME devices) or the so-called P2 connector.

The 743i and 744 SBCs feature a small set of expansion cards, which plug into the available expansion slots and include GSC-mezzanine (GSC-M) and PCI-mezzanine (PMC) cards. It is also possible to use an EISA or PCI cage on several of HP's own systems based on the 743i and 744. Since the board also features an VME controller it can talk to and control other VME cards on the same VME bus/cage. Of note is that some of the pins on the P2-VME connector on the rear are used to route GSC bus traffic to several of the expansion options. VME cages need to be properly jumpered to support this in order to not interfere with these transfers. Also, it is dangerous to use these boards in a VXI cage since some of the VXI pins carry voltage which would result in damaged devices on the GSC bus.

The 743i is technically based on the design of the HP 9000/715 workstations, the 744 partially on the B132L/B160L workstations.

The 743i boards are used in the 748i industrial workstations, the 744 boards in the 745 and 748 industrial workstations.

4.10.2 Internals

CPU

- ◇ 743i/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 743i/100: PA-7100LC 100MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 744/132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 cache
- ◇ 744/165L: PA-7300LC 165MHz with 64/64KB on-chip I/D L1 and 512KB off-chip unified I/D L2 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Wax chip

- EISA bus converter (GSC-to-EISA)
- Second RS232 serial
- ◇ Dino GSC-to-PCI bridge
- ◇ 744: Phantom PseudoBC GSC+ port
- ◇ 744: Visualize-EG (“Graffiti”) graphics
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ VME controller
- ◇ PCMCIA controller

Buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 743i and 744 use different cards
- ◇ 743i: 8-64MB special ECC mezzanine cards
- ◇ 744: 16-256MB special ECC mezzanine cards
- ◇ Up to four cards
- ◇ 743i: 8MB minimum, 256MB maximum amount of RAM
- ◇ 744: 16MB minimum, 1GB maximum amount of RAM

Expansion

- ◇ Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit **or**
- ◇ Two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board
(two additional PMC sites can be obtained through the addition of the A4509A PMC Expander board to the above)

4.10.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ Two micro-DB9 male RS232C serial (*See Note 1*)

- ◇ Micro-DB25 female parallel (*See Note 1*)
- ◇ Micro-DB15 15-pin AUI 10Mbit Ethernet (*See Note 1*)
- ◇ Micro-DB15 VGA graphics (*See Note 1*)
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout (*See Note 1*)

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

4.10.4 ROM update

There is an firmware update available for the 744, which contains the latest version (4.4).

- ◇ PF_C7440044.txt²⁷ has details about the contents and installation of the patch.
- ◇ PF_C7440044²⁸ contains the patch.

4.10.5 References

Manuals

- ◇ 743 Owner's Guide²⁹ (PDF, 1.8MB)
- ◇ 743, 744 and 748 Technical Reference Manual³⁰ (PDF, 2.2MB)
- ◇ 744 Owner's Guide³¹ (PDF, 1.4MB)
- ◇ HP Model 744 Service Handbook³² (.pdf)
- ◇ Installing the A4505A PCI Module Upgrade³³ (PDF, 0.3MB)
- ◇ Installing the A4504A PMC Bridge Adapter and A4509A Expansion Adapter³⁴ (PDF, 0.6MB)
- ◇ Installing Model 743 RAM Boards³⁵ (PDF, 0.2MB)
- ◇ Installing Model 744 RAM Cards³⁶ (PDF, 0.3MB)
- ◇ VME Services for HP-UX 10 and 11³⁷ (PDF, 1.3MB)

²⁷ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044.txt

²⁸ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044

²⁹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38556/lpv38556.pdf>

³⁰ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00265/lpv00265.pdf>

³¹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00271/lpv00271.pdf>

³² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00272/lpv00272.pdf>

³³ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00284/lpv00284.pdf>

³⁴ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00276/lpv00276.pdf>

³⁵ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00298/lpv00298.pdf>

³⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00274/lpv00274.pdf>

³⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00267/lpv00267.pdf>

4.10.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs nicely.
 - 11.00 and 11i: runs nicely.
- ◇ Linux: should run.
- ◇ OpenBSD: should run.

4.10.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
743i/64	2.52	3.31
743i/100	3.76	4.03
744/123L	6.45	6.70
744/165L	7.90	7.64

4.11 HP 9000/745 VME Workstations

4.11.1 Overview

The 745 *industrial systems* are 744 VME boards in a heavy VME case, which provides the necessary I/O facilities:

- ◇ Room for up to four SCSI devices, which can be accessed from the outside
- ◇ Four-slot EISA or PCI cage
- ◇ Room for PCI-mezzanine expansion cards, via special PMC bridges/expansion

4.11.2 Internals

CPU

- ◇ 745/132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 cache
- ◇ 745/165L: PA-7300LC 165MHz with 64/64KB on-chip I/D L1 and 512KB off-chip unified I/D L2 cache

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
- ◇ Dino GSC-to-PCI bridge (on the PMC expansion adapter?)
- ◇ Phantom PseudoBC GSC+ port
- ◇ Visualize-EG (“Graffiti”) graphics
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ VME controller (“Backplane controller ASIC”)
- ◇ PCMCIA controller

Buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 16-256MB special ECC mezzanine cards (same as for the 744 VME boards)
- ◇ Up to four cards can be installed
- ◇ 16MB minimum, 1GB maximum amount of RAM

Expansion

- ◇ Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit or
- ◇ Two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board (two additional PMC sites can be obtained through the addition of the A4509A PMC Expander board to the above). The PMC bridge/expander boards connect to the VME backplane on a VME slot above the 744 processing board. However they probably use the GSC bus routed through the VME P1/P2 connectors, and not the VME bus.
- ◇ Either four EISA or four PCI (5V) slots in a separate I/O cage

Drives

- ◇ Four bays for external-accessible SCSI (SCSI-2 Single-ended) drives
- ◇ One bay for a 3.5" SCSI drive

4.11.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ Two Micro-DB9 male RS232C serial (*See Note 1*)
- ◇ Micro-DB25 female parallel (*See Note 1*)
- ◇ Micro-DB15 15-pin AUI 10Mbit Ethernet (*See Note 1*)
- ◇ Micro-DB15 VGA graphics (*See Note 1*)
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout (*See Note 1*)

Notes

- 1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

4.11.4 ROM update

There is an firmware update available for the 744 VME boards which contains the latest version (4.4).

- ◇ PF_C7440044.txt³⁸ has details about the contents and installation of the patch.
- ◇ PF_C7440044³⁹ contains the patch.

4.11.5 References

Manuals

- ◇ HP Model 745 Technical Reference Manual⁴⁰ (.pdf) Hewlett Packard (April 1999, edition E1199, part number A4964-90603)
- ◇ Model 745 Industrial Controller Owner's Guide⁴¹ (.pdf) Hewlett Packard (April 1999, edition E0499, part number A4964-90604)
- ◇ Model 745 Service Handbook⁴² (.pdf) Hewlett Packard (November 1999, edition E1199, part number A4964-90602)

Other

- ◇ Refer also to the 743i and 744 VME boards description

4.11.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works
 - 10.20: runs very nice
 - 11.00 and 11i: runs nice, needs properly at least 256MB RAM
- ◇ Linux: should run
- ◇ OpenBSD: should run

4.11.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
745/123L	6.45	6.70
745/165L	7.90	7.64

³⁸ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044.txt

³⁹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044

⁴⁰ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00264/lpv00264.pdf>

⁴¹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00294/lpv00294.pdf>

⁴² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00279/lpv00279.pdf>

4.11.8 Physical dimensions/Power

- ◇ 177×425×412mm height/width/depth
- ◇ 29.0kg weight
- ◇ 400W power supply

4.12 HP 9000/745i & 747i VME Workstations

4.12.1 Overview

These *Pace* named models were one of the first PA-RISC workstations for industrial/medical use. They are technically very similar to the older 715 workstations and 725 workstations while being built in ruggedized, rack-mountable cases. The CPU and I/O controllers sit on a VME SBC (single board computer) which is identical on both 745i and 747i. The latter systems are built in an even bigger case and feature VME slots, which the 745i do not have. Both have a HP-IB interface, which was used mainly for controlling and/or instrumental use. Interestingly these machines have two pairs of LED banks, one at the front and the other directly on the CPU board on the back.

4.12.2 Internals

CPU

- ◇ 745i/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- ◇ 747i/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- ◇ 745i/100: PA-7100 100MHz with 256/256KB off-chip I/D L1 cache
- ◇ 747i/100: PA-7100 100MHz with 256/256KB off-chip I/D L1 cache

Chipset

- ◇ ASP chipset, featuring:
 - NCR 53C700 8-bit single-ended SCSI-2
 - Intel 82596DX 10Mb Ethernet controller
 - WD 16C552 parallel
 - NS 16550A compatible serial
 - 512KB EPROM - the Boot ROM
 - 8KB EEPROM for storing system configuration status etc.
 - Intel 8042 microprocessor controlling:
 - * battery backed RTC
 - * system & user timers
 - * audio generator
 - * HP-HIL interface
 - * frontpanel system status LEDs
- ◇ Viper memory and I/O controller
- ◇ Intel 82501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)

- ◇ CRX graphics, 8-bit
- ◇ HP-IB controller
- ◇ 747i: VME controller
- ◇ PSB2160 CODEC for 8-bit mono audio

Buses

- ◇ PBus processor/memory bus
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus
- ◇ EISA I/O expansion bus
- ◇ HP-IB bus (IEEE-488); peripheral bus
- ◇ SCSI-2 narrow single-ended bus
- ◇ 747i: SGC expansion of the mainbus to the SGC expansion slot
- ◇ 747i: VME bus

Memory

- ◇ 72-pin ECC SIMM
- ◇ 8-32MB modules (/100 models take 64MB modules)
- ◇ Four sockets
- ◇ /50 models: 16MB (2×8) minimum, 128MB (4×32) maximum
- ◇ /100 models: 16MB (2×8) minimum, 256MB (4×64) maximum

Expansion

- ◇ 745i:
 - Four EISA expansion slots
- ◇ 747i:
 - Two EISA expansion slots
 - One SGC (*DIO-II formfactor*) expansion slot
 - Six VME slots

Drives

- ◇ One bay for an external-accessible 5.25" half-height SCSI drive
- ◇ One bay for an external-accessible 3.5" SCSI drive or floppy

- ◇ One bay for a 3.5" SCSI drive

4.12.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ HD 15 VGA
- ◇ HP-HIL connector for input devices
- ◇ HP-IB for peripherals
- ◇ Three phone jacks (microphone-in, headphone-out and speaker-out)

4.12.4 References

Manuals

- ◇ **Models 745i/50, 745i/100, 747i/50, and 747i/100 Owner's Guide**⁴³ (.pdf) Hewlett Packard (August 1993: First edition, part-number A2628-90014)

4.12.5 Operating systems

- ◇ HP-UX: every release from 10.01-10.20 works.
 - 10.20: runs nice on them.
 - 11.00: also works, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- ◇ NeXTSTEP: Version 3.3 could work.
- ◇ Linux: works.
- ◇ OpenBSD: works.

4.12.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
/50	36	72	1.53	2.46
/100	81	138	3.22	4.06

4.12.7 Physical dimensions/Power

745i:

⁴³ <http://bizsupport2.austin.hp.com/bc/docs/support/SupportManual/lpv00303/lpv00303.pdf>

- ◇ 175×425×412mm height/width/depth
- ◇ 18.6kg net weight
- ◇ 350W max. power input

747i:

- ◇ 310×425×412mm height/width/depth
- ◇ 29kg net weight
- ◇ 700W max. power input

4.13 HP 9000/748i & 748 VME Workstations

4.13.1 Overview

The 748i and 748 *ruggedized workstations* are 743i and 744 VME boards in a heavy, large VME-case, which provides the necessary I/O facilities:

- ◇ Six 6U VME slots for additional I/O boards
- ◇ Room for up to four SCSI devices, which can be accessed from the outside
- ◇ Four-slot EISA or PCI cage

4.13.2 Internals

CPU

- ◇ 748i/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 748i/100: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ◇ 748/132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 cache
- ◇ 748/165L: PA-7300LC 165MHz with 64/64KB on-chip I/D L1 and 512KB off-chip unified I/D L2 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
- ◇ Dino GSC-to-PCI bridge
- ◇ 748: Phantom PseudoBC GSC+ port
- ◇ 748: Visualize-EG (“Graffiti”) graphics
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ VME controller

- ◇ PCMCIA controller

Buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 748i and 748 use different cards
- ◇ 748i: 8-64MB special ECC mezzanine cards
- ◇ 748: 16-256MB special ECC mezzanine cards
- ◇ Up to four cards
- ◇ 748i: 8MB minimum, 256MB maximum amount of RAM
- ◇ 748: 16MB minimum, 1GB maximum amount of RAM

Expansion

- ◇ Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit or
- ◇ Two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board (two additional PMC-sites can be obtained through the addition of the A4509A PMC Expander board to the above)
- ◇ Six 6U VME slots
- ◇ Either four EISA or four PCI slots in a separate I/O cage

4.13.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ Two Micro-DB9 male RS232C serial (*See Note 1*)
- ◇ Micro-DB25 female parallel (*See Note 1*)
- ◇ Micro-DB15 15-pin AUI 10Mbit Ethernet (*See Note 1*)
- ◇ Micro-DB15 VGA graphics (*See Note 1*)
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout (*See Note 1*)
- ◇ On configurations with an EISA cage: HIL connector

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

4.13.4 ROM update

There is an firmware update available for the 744-board (used in 748), which contains the latest version (4.4).

- ◇ PF_C7440044.txt⁴⁴ has details about the contents and installation of the patch.
- ◇ PF_C7440044⁴⁵ contains the patch.

4.13.5 References

Manuals

- ◇ Model 748 Workstation Owner's Guide⁴⁶ (PDF, 3.2MB)
- ◇ Service Handbook Model 748⁴⁷ (PDF, 3.6MB)

Other

- ◇ Refer also to the 743i and 744 workstations

4.13.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works
 - 10.20: runs very nice
 - 11.00 and 11i: runs nice, needs properly at least 256MB RAM
- ◇ Linux: should run
- ◇ OpenBSD: should run

4.13.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
748i/64	2.52	3.31
748i/100	3.76	4.03
748/123L	6.45	6.70
748/165L	7.90	7.64

⁴⁴ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044.txt

⁴⁵ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044

⁴⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00281/lpv00281.pdf>

⁴⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00282/lpv00282.pdf>

4.13.8 Physical dimensions/Power

- ◇ 324×425×419mm height/width/depth
- ◇ 29.0kg weight
- ◇ Two redundant 350W power supplies

4.14 HP 9000 74x Expansion

4.14.1 743i and 748i (/64 and /100) RAM

Used in:

- ◇ 743i/{64,100}
- ◇ 748i/{64,100}

HP parts:

- ◇ A4263A - 8MB RAM card
- ◇ A4264A - 16MB RAM card
- ◇ A4265A - 32MB RAM card
- ◇ A4266A - 64MB RAM card

4.14.2 744, 745 and 748 (/132L and /165L) RAM

Used in:

- ◇ 744/{132L,165L}
- ◇ 745/{132L,165L}
- ◇ 748/{132L,165L}

Faster versions of the above 743i/748i ECC mezzanine cards.

Original HP part numbers:

- ◇ A4501A - 16MB RAM card (only supported in HP-RT)
- ◇ A4502A - 32MB RAM card
- ◇ A4503A - 64MB RAM card
- ◇ A4449A - 128MB RAM card
- ◇ A6005A - 256MB RAM card

4.14.3 Cables

Breakout cables for the micro-connectors found on the 743i and 744 VME boards. These cables convert the micro-output to the regular connectors.

- ◇ HP A4300A HP Parallel: High Density 25-pin to standard 25-pin (female)
- ◇ HP A4301A RS-232C: High Density 9-pin to standard 9-pin (male)
- ◇ HP A4302A Audio: High Density 9-pin to three mini jacks

- ◇ HP A4303A LAN: High Density 15-pin to 15-pin AUI
- ◇ HP A4305A Video for EVC monitors: High Density 15-pin to EVC 35-pin connector (female)
- ◇ HP A4223A Video: High Density 15-pin to standard 15-pin (female)
- ◇ HP C2955A SCSI: High Density 50-pin to High Density 50-pin, .5m (male)

4.14.4 GSC-M cards

GSC-M cards are special mezzanine versions of expansion cards for the GSC bus.

- ◇ A4267A - 8-plane graphics
- ◇ A4268A - Fast-Wide *high-voltage differential* (HVD) SCSI
- ◇ A4315A - HCRX-8 graphics
- ◇ A4316A - HCRX-24 graphics
- ◇ J3420A - ATM card

4.15 HP 9000/A180

4.15.1 Overview

The PA-7300LC A180 and A180C were some of the latest 32-bit PA-RISC HP 9000 servers. They are quite small and rack-mountable. Designated “Enterprise Internet Servers” they do not have any video output, only serial console and *Secure Web Console*.

Introduced: September 1998, discontinued: February 2001

4.15.2 Internals

CPU

- ◇ A180: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 cache
- ◇ A180C: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 and 1MB off-chip unified L2 cache

The additional 1MB L2 cache is the only difference between both systems. This cache is upgradeable through two DIMM slots near the CPU.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - NS 16550A compatible serial
- ◇ Dino GSC-to-PCI bridge
- ◇ Phantom PseudoBC GSC+ port
- ◇ DEC 21142/43 10/100BaseT PCI Ethernet

Buses

- ◇ GSC+ general system-level I/O bus (probably clocked at 36MHz — 144MB/s peak data rate)
- ◇ PCI high performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended; main storage I/O bus

Memory

- ◇ 72-pin ECC EDO SIMMs, 60ns or faster.
- ◇ Takes 64-256MB modules
- ◇ Eight slots
- ◇ 128MB (2×64) minimum, 2048MB (8×256) maximum

Expansion

- ◇ Two slots for either GSC (*EISA formfactor*) or PCI cards

Drives

- ◇ One tray for two 3.5" Fast-Narrow 50-pin SCSI hard drives

4.15.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ DB9 male RS232C serial
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ TP/RJ45 10Mbit Ethernet "Web Console"

4.15.4 References

Manuals

- ◇ A180 User's Manual⁴⁸ (PDF, 0.9MB)

4.15.5 ROM update

There is a firmware update available for the A180[C], which contains the latest version (39.32).

- ◇ PF_CSTD3932.txt⁴⁹ has details about the contents and installation of the patch.
- ◇ PF_CSTD3932⁵⁰ contains the patch.

4.15.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs very nice
 - 11.00 and 11i v1: run nice
- ◇ Linux: works fine.
- ◇ OpenBSD: works fine.
- ◇ NetBSD: experimental support as of 5/2005.

4.15.7 Benchmarks

⁴⁸ <http://docs.hp.com/hpux/pdf/Aclassdocoo.pdf>

⁴⁹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CSTD3932.txt

⁵⁰ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CSTD3932

Model	SPEC95, int	SPEC95, fp
A180	?	?
A180C	9.22	8.60

4.16 HP A400 & A500 (rp2400/rp2430 & rp2450/rp2470)

4.16.1 Overview

The rp2400/rp2430 (A400) and rp2450/rp2470 (A500) are the 64-bit successors of the popular A180 rack servers. The chassis is similar—still 2U rack-mountable—but the interior changed significantly. The various A400/A500 models have various 64-bit PA-RISC processors with large on-chip L1 caches. The I/O subsystem is based on Astro memory/CPU controller and several Elroy PCI bridges for the various PCI slots and integrated I/O devices. The difference between the A400 and A500 is that the latter are SMP-capable and can use more memory modules and PCI cards.

They feature an advanced version of the *Secure Web Console* found in the earlier A180 systems. Called “Guardian Service Processor” (GSP) it can be reached with pressing **Ctrl-b**. It can be used for a wide range of administrative tasks; in the References section is a link to a detailed command summary.

Introduced: May 2000, discontinued: September 2002, with prices of the entry version of \$4,600 for the A400-44 and \$9,200 for a single-CPU A500-5X.

Model numbers:

- ◇ A400-36, A400-44, A400-5X: rp2400
- ◇ A400-6X, A400-7X: rp2430
- ◇ A500-36, A500-44, A500-5X: rp2450
- ◇ A500-6X, A500-7X: rp2470

4.16.2 Internals

CPU

The A400 systems are uniprocessor systems while the A500 support up to 2-way SMP. The A400 (rp2400/rp2430) and A500 (rp2450/rp2470) are based on a different system boards, which supported different types of processors:

- ◇ A400/rp2400 — A6109A, A6109B: one 440MHz processor
- ◇ A400/rp2430 — A6890A: one 650MHz processor [probably supports 550MHz too]
- ◇ A500/rp2450 — A5570A, A5570B, A8329A: up to two 440MHz or 550MHz processors
- ◇ A500/rp2470 — A6890A: up to two 650MHz or 750MHz processors

The following table lists the various suffixes denoting the different theoretically possible CPU configurations. Upgrading from one configuration to another could require the replacement of other parts besides the processor, *e.g.*, the mainboard or power supply.

- ◇ -44: PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each [A400/rp2400, A500/rp2450]
- ◇ -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each [A500/rp2450, A400 probably too]
- ◇ -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each [A400/rp2430, A500/rp2470]
- ◇ -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each [A500/rp2470]

- ◇ Unsure if the following two processors were ever actually supported/shipped:
- ◇ -8X: PA-8700 875MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -9X: PA-8800 (dual-core) 900MHz/1.0GHz with 1.5/1.5MB on-chip L1 and 32MB off-chip L2 cache each

Chipset

- ◇ Astro memory/Runway controller, connects to the system/processor bus (1-2 CPUs), dedicated memory bus and to the I/O systems via five (A400) or seven (A500) I/O links
- ◇ rp2430 (A400): Three Elroy PCI bridges (LBAs), convert the five I/O links from Astro into three PCI buses
- ◇ rp2470 (A500): Four Elroy PCI bridges (LBAs), convert the seven I/O links from Astro into four PCI buses
- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C876 SCSI controller, (includes 2 Symbios Logic 53C875 cores with each one Ultra-Wide SCSI-2 bus)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- ◇ Runway CPU/memory bus, 120MHz
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD buses
- ◇ rp2430 (A400):
 - 1.9GB/s system bus bandwidth
 - 1.3GB/s I/O bus bandwidth (five 250MB/s I/O links)
 - 1.9GB/s memory bandwidth
 - Three independent PCI-64/66 I/O buses (on five I/O links):
 1. PCI-64/66 bus on two I/O links (500MB/s) for one PCI “Twin-turbo” slot (slot 1)
 2. PCI-64/66 bus on two I/O links (500MB/s) for one PCI “Twin-turbo” slot (slot 2)
 3. PCI-64/66 bus on one I/O link (250MB/s) for the core I/O — SCSI, Ethernet networking, management LAN, serial ports, etc.
- ◇ rp2470 (A500):
 - 1.9GB/s system bus bandwidth
 - 1.9GB/s I/O bus bandwidth (seven 250MB/s I/O links)
 - 1.9GB/s memory bandwidth

- Four independent PCI-64/66 I/O buses (on seven I/O links):
 1. PCI-64/66 bus on two I/O links (500MB/s) for one PCI “Twin-turbo” slot (slot 1)
 2. PCI-64/66 bus on two I/O links (500MB/s) for one PCI “Twin-turbo” slot (slot 2)
 3. PCI-64/66 bus on two I/O links (500MB/s) for two PCI “shared” slots (slot 3 and 4)
 4. PCI-64/66 bus on one I/O link (250MB/s) for the core I/O — SCSI, Ethernet networking, management LAN, serial ports, etc.

Memory

- ◇ ECC SDRAM DIMMs
- ◇ Take 256MB/512MB/1GB modules
- ◇ Eight slots, A400 can only use first 4 of those
- ◇ 256MB (1×256) minimum, A400/rp2430: 2GB (4×512MB) maximum, A500/rp2470: 8GB (8×1GB) maximum

Expansion

- ◇ A400/rp2430: Two PCI 64-bit/66MHz, 5V slots [two slots from the A500 are disabled]
- ◇ A500/rp2470: Four PCI 64-bit/66MHz, 5V slots
- ◇ Two of those slots are “Twin-turbo” slots (slot 1 and 2), each on its own dedicated PCI bus connected via two dedicated 250MB/s I/O channel (rope)
- ◇ A500/rp2470: The other two slots are “shared” slots (slots 3 and 4) and share two 250MB/s I/O channels—if only one slot is used it is allocated two channels and becomes a “Twin-turbo” slot in effect

Drives

- ◇ Two trays for each one 3.5” Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector which require a special spud to be plugged into the system.

4.16.3 External connectors

- ◇ 50-pin HD SCSI-2 Ultra-Narrow single-ended
- ◇ 68-pin HD SCSI-3 Ultra2-Wide LVD
- ◇ DB25 male RS232C serial for console/UPS (a break-out cable which converts to three DB9 plugs)
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ TP/RJ45 10Mbit Ethernet for Secure Web Console/GSP

4.16.4 ROM update

There is an firmware update available which contains the latest version (43.50).

- ✧ PF_CHAW4350.txt⁵¹ has details about the contents and installation of the patch.
- ✧ PF_CHAW4350.tar.gz⁵² contains the patch.

There is also an firmware update available for revision B GSP service processors on rp2430 and rp2470 systems which contains the latest version C.02.14.

- ✧ PF_CHARGSPCo214.txt⁵³ has details about the contents and installation of the patch.
- ✧ PF_CHARGSPCo214.tar.gz⁵⁴ contains the patch.

There is also an firmware update available for revision A GSP service processors on rp2430 and rp2470 systems which contains the latest version A.01.12.

- ✧ PF_CPREGSPA0112.txt⁵⁵ has details about the contents and installation of the patch.
- ✧ PF_CPREGSPA0112.tar.gz⁵⁶ contains the patch.

4.16.5 References

Manuals

- ✧ *hp server rp2400 series whitepaper*, Hewlett-Packard Company (February 2002, product number 5981-0175EN) [did not find an appropriate URL for this PDF document — *Ed.*]
- ✧ *rp24xx Hardware Manual*⁵⁷ (PDF) Hewlett-Packard Company (n. d.)

Website

- ✧ *Doug's HP 9000 - GSP Notes Page*⁵⁸ with a detailed description of the available GSP commands.

4.16.6 Operating systems

- ✧ HP-UX: Only 64-bit 11.00 and 11i (v1 and v2) releases run.
- ✧ Linux: works, but the SMP support on some models supposedly is a bit flaky and not all CPU configurations are supported.

⁵¹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHAW4350.txt

⁵² ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHAW4350.tar.gz

⁵³ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHARGSPCo214.txt

⁵⁴ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHARGSPCo214.tar.gz

⁵⁵ ftp://ftp.itrc.hp.com/archived_patches/firmware_patches/hp/cpu/PF_CPREGSPA0112.txt

⁵⁶ ftp://ftp.itrc.hp.com/archived_patches/firmware_patches/hp/cpu/PF_CPREGSPA0112.tar.gz

⁵⁷ http://www.docs.hp.com/hpux/onlinedocs/2411/rp24xx_customer.pdf

⁵⁸ <http://web.tampabay.rr.com/batcave/GSPinfo.htm>

4.16.7 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
A500-5X(rp2450)	422	414	2-CPU: 9.3	2-CPU: 7.6
A500-7X(rp2470)	581		6.74 2-CPU: 12.9	

4.16.8 Physical dimensions/Power

- ◇ 95×482×635 mm height/width/depth
- ◇ rack-mounted: 2U height, 482×774 mm width/depth
- ◇ 22.68kg net weight

4.17 HP Visualize B132L, B160L & B180L

4.17.1 Overview

These are very nice, small entry-level workstations. Still based on a 32-bit PA-RISC CPU they were designed as successors to the successful 715 workstations with better performance and I/O-expandability. They were developed alongside the C-Class workstations, sharing a similar casing concept but integrating more functionality onto a single mainboard to save manufacturing costs. The +-models (B132L+, B180L+) differ from the others in having Ultra-Wide SE SCSI and 10/100Mb Ethernet rather than Fast-Wide HVD SCSI and only 10Mb Ethernet.

Several B132L and B160L models feature a faulty PCI backplane chip (Dino), which could result in data loss. A firmware patch in PDC version 6.1 added a check for the faulty chip—if such a chip is found, subsequent PCI cards in the PCI slots in question are disabled and the system halts a boot-up/PDC.

Model numbers: all have the HP 9000/778 model number.

4.17.2 Internals

CPU

- ◇ B132L: PA-7300LC 132MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- ◇ B132L+: PA-7300LC 132MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- ◇ B160L: PA-7300LC 160MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- ◇ B180L+: PA-7300LC 180MHz with 64/64KB int. L1 (+ 1MB ext. L2)

The external L2 cache SRAM is optional and is installed in two DIMM slots below the CPU socket. The modules must be of equal size. Usually, these systems come with 2 512KB modules, totalling in 1MB L2.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
- ◇ Dino GSC-to-PCI bridge
- ◇ Phantom PseudoBC GSC+ port

- ◇ Visualize-EG (“Graffiti”) graphics
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ B132L, B160L: NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- ◇ B132L+, B180L+: Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- ◇ B132L+, B180L+: DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- ◇ GSC general system-level I/O bus
 - B132L (both): 33MHz 132MB/s
 - B160L: 40MHz 160MB/s
 - B180L+: 36MHz 144MB/s
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ B132L, B160L: SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus
- ◇ B132L+, B180L+: SCSI-2 Ultra-Wide single-ended main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Takes 16-256MB modules (latest firmware-rev needed)
- ◇ Six slots
- ◇ 32MB (2×16) minimum, 1.5GB (6×256) maximum

Expansion

- ◇ B132L, B160L:
 - One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 3.3V card
 - One slot for either a GSC (*EISA formfactor*), PCI 32-bit/33MHz, 3.3V or EISA card
- ◇ B132L+, B180L+:
 - One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 5V card
 - One slot for either a GSC (*EISA formfactor*), PCI 32-bit/33MHz, 5V or EISA card
- ◇ I/O slot layout (from top to bottom):

1. PCI-32/33 or GSC
2. PCI-32/33 or EISA or GSC

Drives

- ◇ One tray for a 68-pin half-height 3.5" SCSI hard drive, either Fast-Wide *high-voltage differential* (B132L, B160L) or Ultra-Wide SE (+-models)
- ◇ One tray for a 3.5" Floppy drive
- ◇ One tray for a 50-pin half-height 5.25" Fast-Narrow 50-pin SE SCSI drive, external accessible, can also accommodate a hard drive.

4.17.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ B132L, B160L: 68-pin HD SCSI-2 Fast-Wide *high-voltage differential*
- ◇ B132L+, B180L+: 68-pin HD SCSI-3 Ultra-Wide single-ended
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ B132L, B160L: TP/RJ45 10Mbit Ethernet
- ◇ B132L+, B180L+: TP/RJ45 10/100Mbit Ethernet
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ EVC graphics port (*See Note 1*)
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.17.4 ROM update

There is an firmware update available for the B-Class, which contains the latest version (6.1).

- ◇ PF_CB1X0061.txt⁵⁹ has details about the contents and installation of the patch.
- ◇ CB1X0061.frm⁶⁰ contains the patch.

⁵⁹ http://ftp.parisc-linux.org/kernels/b180/PF_CB1X0061.txt

⁶⁰ <http://ftp.parisc-linux.org/kernels/b180/CB1X0061.frm>

4.17.5 References

Manuals

- ◇ B-Class Owner's Guide⁶¹ (PDF, 1.5MB)
- ◇ B-Class Service Handbook⁶² (PDF, 0.9MB)

Articles

- ◇ A Low-Cost Workstation with Enhanced Performance and I/O Capabilities⁶³ (.pdf) Scott P. Allan et al (June 1997: Hewlett-Packard Journal)

4.17.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs very nicely.
For a B180L+ you need at least ACE 9707
 - 11.00 and 11.11 v1 (B180L: v1 September 2005 last officially supported; all others: v1 December 2004): run nicely.
- ◇ Linux: works fine.
- ◇ OpenBSD works fine (the 53C720 Fast-Wide HVD SCSI controller on B132L and B160L is supported since release 4.2).
- ◇ NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI controller found on the B132L and B160L is not supported.

4.17.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
B132	6.45	6.70	58.1	60.3
B132+	6.84	7.17	61.5	64.6
B160L	7.75	7.56	69.7	68.1
B180L+	9.22	9.43	83.0	84.8

4.17.8 Physical dimensions/Power

- ◇ 116×445×452 mm height/width/depth
- ◇ 16kg net weight, 18kg fully loaded
- ◇ 300W max. power input
- ◇ 3A max. RMS at 240V
- ◇ 5A max. RMS at 120V

⁶¹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37741/lpv37741.pdf>

⁶² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37927/lpv37927.pdf>

⁶³ <http://www.hpl.hp.com/hpjournal/97jun/jun97a11.pdf>

4.18 HP Visualize B2000 & B2600

4.18.1 Overview

These workstations were aimed at the graphics workstations market, equipped with the 64-bit PA-8500 or PA-8600 featuring large on-chip L1 caches. The B2000 features normally the former CPU and is shipped in a small tower enclosure whereas the B2600 is shipped in a desktop casing, featuring the PA-8600 CPU. The architecture was a major change from those of its predecessors, *e.g.*, the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports.

Model numbers: both the B2000 and B2600 have the HP 9000/785 model number.

4.18.2 Internals

CPU

- ◇ B2000: PA-8500 400MHz with 512/1024KB on-chip I/D L1 cache

- ◇ B2600: PA-8600 500MHz with 512/1024KB on-chip I/D L1 cache

(there are some B2000s shipped with/upgraded to PA-8600 (PCXW+) processors)

Chipset

- ◇ Astro memory/Runway controller

- ◇ Two Elroy PCI bridges

- ◇ National 87560 (SuperI/O), handling USB, RS232, parallel, floppy and IDE

- ◇ National 87415 IDE controller

- ◇ National USB controller

- ◇ Analog Devices AD1889 sound chip (on B2600 the audio card is optional)

- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)

- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

- ◇ B2000: Visualize FXe graphics

Buses

- ◇ Runway CPU/memory bus

- ◇ PCI-32/33 device I/O bus

- ◇ PCI-64/33 high-performance I/O bus

- ◇ SCSI-3 Ultra2-Wide LVD bus main storage I/O

- ◇ IDE bus; removable device-I/O (can partially boot from CD-ROM, *e.g.*, HP-UX)

Memory

- ◇ 278-pin 120MHz ECC SD-RAM DIMMs
- ◇ Takes 128MB-1GB modules
- ◇ Four slots
- ◇ 128MB (1×128) minimum, 4GB (4×1GB) maximum

Expansion

- ◇ Two PCI 64-bit/33MHz, 5V slots (clocked at 66MHz on B2600)
- ◇ Two PCI 32-bit/33MHz, 5V slots
- ◇ B2000 I/O slot layout (from top to bottom):
 1. PCI-64/33, 5V
 2. PCI-64/33, 5V
 3. PCI-32/33, 5V
 4. PCI-32/33, 5V
- ◇ B2600 I/O slot layout (from top to bottom):
 1. PCI-32/33, 5V, short PCI cards
 2. PCI-32/33, 5V, short PCI cards
 3. PCI-64/33, 5V, short and full-length cards
 4. PCI-64/33, 5V, short and full-length cards

Drives

- ◇ One tray for two 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector
- ◇ One tray for a 3.5" Floppy drive
- ◇ One tray for a half-height 5.25" IDE drive, external accessible

4.18.3 External connectors

- ◇ B2000: HD15 VGA
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ Two USB ports for keyboard & mouse
- ◇ Four audio jacks (microphone, headphones, line-in and line-out) (on B2600 the audio card is optional)

4.18.4 ROM update

There is an firmware update available for the B2000, which contains the latest version (5.0).

- ✧ PF_CBCJ0050.txt⁶⁴ has details about the contents and installation of the patch.
- ✧ PF_CBCJ0050⁶⁵ contains the patch.

4.18.5 References

Manuals

- ✧ B2000 Service Handbook⁶⁶ (PDF, 8.8MB)
- ✧ B2000 Owner's Guide⁶⁷ (PDF, 2.6MB)
- ✧ B2600 Technical Reference Manual⁶⁸ (PDF, 33.0MB)
- ✧ VISUALIZE Workstation Memory Subsystem⁶⁹ (PDF, 120KB)

4.18.6 Operating systems

- ✧ HP-UX:
 - B2000: 10.20 ACE 9912 (unclear if B2600 supports 10.20)
 - 11.00 minimum EP 9808 or ACE 9911 and 11i v1
- ✧ Linux: works.
- ✧ OpenBSD (32-bit): works.

4.18.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95 rate, int	SPEC95 rate, fp	SPEC2000, int	SPEC2000, fp	SPEC2000 rate, int	SPEC2000 rate, fp
B2000	31.80	52.40	286	472	332	357	3.8	4.1
B2600					403	440	4.7	5.1

4.18.8 Physical dimensions/Power

B2000:

- ✧ 445×229×495 mm height/width/depth
- ✧ rack-mounted: 6U height, 451×665 mm width/depth
- ✧ 18.6kg net weight, 21.4kg fully loaded

⁶⁴ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt

⁶⁵ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050

⁶⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37671/lpv37671.pdf>

⁶⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37670/lpv37670.pdf>

⁶⁸ <http://bizsupport1.austin.hp.com/bc/docs/support/SupportManual/lpv38329/lpv38329.pdf>

⁶⁹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf>

- ◇ 620W max. power input
- ◇ 3.5A max. RMS at 240V
- ◇ 8.0A max. RMS at 120V

B2600:

- ◇ 127×425×457 mm height/width/depth
- ◇ rack-mounted: 127×483×495 mm width/depth
- ◇ 18.2kg net weight, 20.2kg fully loaded
- ◇ 1.8A max. RMS at 240V
- ◇ 3.6A max. RMS at 120V

4.19 HP 9000/C100 & C110

4.19.1 Overview

The C100 and C110 are graphics workstations with the PA-7200 processors. They have a similar case to that of the old 735 — built of interlocking modules of the I/O and MPU board.

Model numbers: both the C100 and C110 have the HP 9000/777 model number.

4.19.2 Internals

CPU

- ◇ C100: PA-7200 100MHz with 256/256KB off-chip I/D L1 cache and 2KB on-chip “assist” L1 cache
- ◇ C110: PA-7200 120MHz with 256/256KB off-chip I/D L1 cache and 2KB on-chip “assist” L1 cache

The “assist” cache is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ U2 I/O adapter Runway to GSC bridge
- ◇ MMC/SMC memory controllers
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP HIL interface
- ◇ GSC graphics
- ◇ Intel 82C503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2

Buses

- ◇ Runway CPU/memory bus (100MHz 800MB/s peak data rate on C100, 120MHz, 960MB/s on C110)
- ◇ GSC general system-level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ 400MB/s (C100), 480MB/s (C110) peak bandwidth
- ◇ Takes 16-128MB modules
- ◇ Eight slots
- ◇ 32MB (2×16) minimum, 1GB (8×128) maximum

Expansion

- ◇ One slot for a GSC (*EISA formfactor*) card
- ◇ Three slots for either GSC (*EISA formfactor*) or EISA cards
- ◇ I/O slot layout (from top to bottom):
 1. EISA or GSC
 2. EISA or GSC
 3. EISA or GSC (for secondary graphics)
 4. GSC (for primary graphics)

Drives

The disk-slider can accommodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- ◇ Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- ◇ One 3.5" Floppy drive and
- ◇ One external-accessible half-height 5.25" SCSI drive (CD/DAT).

4.19.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- ◇ Two DB9 male RS232C serial (up 460.8Kb/s)
- ◇ DB25 female parallel
- ◇ TP/RJ45 10Mbit Ethernet
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ Graphics port depend on installed video adapter
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)

4.19.4 ROM update

There is a firmware update available for the C110, which contains the latest version (1.3).

- ◇ PF_CC110013.txt⁷⁰ has details about the contents and installation of the patch.
- ◇ PF_CC110013⁷¹ contains the patch.

There is also a firmware update available for the C100 and C110, which contains the latest version (1.2).

- ◇ PF_CC1X0012.txt⁷² has details about the contents and installation of the patch.
- ◇ PF_CC1X0012⁷³ contains the patch.

4.19.5 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs very nicely.

⁷⁰ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC110013.txt

⁷¹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC110013

⁷² ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC1X0012.txt

⁷³ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC1X0012

- 11.00 and 11i: runs nicely
- ◇ Linux: works fine.
- ◇ OpenBSD works fine (the 53C720 Fast-Wide HVD SCSI controller is supported since release 4.2).

4.19.6 References

Manuals

- ◇ C100/110 Owners Guide⁷⁴ (PDF, 1.6MB)
- ◇ C100/110 Service Handbook⁷⁵ (PDF, 1.5MB)
- ◇ C100 to C110 CPU upgrade⁷⁶ (PDF, 0.2MB)
- ◇ C100, C110 to C160L CPU upgrade⁷⁷ (PDF, 0.5MB)
- ◇ C100, C110 to C160, C180 CPU upgrade⁷⁸ (PDF, 0.5MB)
- ◇ C100, C110, C160, C180 to C200 CPU upgrade⁷⁹ (PDF, 0.5MB)

4.19.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPeCrate95, int	SPeCrate95, fp
C100	4.98	6.59	44.8	59.4
C110	6.00	8.14	54.0	73.3

4.19.8 Physical dimensions/Power

- ◇ 138×539×447 mm height/width/depth
- ◇ 16.7kg net weight, 21.1kg fully loaded
- ◇ 555W max. power input
- ◇ 5.0A max. RMS at 240V
- ◇ 9.5A max. RMS at 120V

⁷⁴ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37672/lpv37672.pdf>

⁷⁵ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37947/lpv37947.pdf>

⁷⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37945/lpv37945.pdf>

⁷⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37952/lpv37952.pdf>

⁷⁸ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37949/lpv37949.pdf>

⁷⁹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf>

4.20 HP Visualize C132L & C160L

4.20.1 Overview

These were entry-level workstations equipped with the low-cost PA-7300LC CPU. They have a similar case to that of the old 735 — built of interlocking modules so the I/O board, MPU board etc. can be easily taken out.

Model numbers: both the C132L and C160L have the HP 9000/779 model number.

4.20.2 Internals

CPU

- ◇ C132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified L2) cache
- ◇ C160L: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified L2) cache

The off-chip L2 cache SRAM is optional and is installed in two DIMM slots below the CPU socket. The modules must be of equal size. Usually, these systems come with 2 512KB modules, totalling in 1MB L2 cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP HIL interface
- ◇ Dino GSC-to-PCI bridge
- ◇ Phantom PseudoBC GSC+ port
- ◇ Visualize-EG graphics
- ◇ Intel 82C503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ NCR 53C720 16-bit Fast-Wide *differential* (HVD) SCSI-2

Buses

- ◇ GSC-2 system and I/O bus (33MHz with 132MB/s peak data rate on C132L, 40MHz 160MB/s on C160L)
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide *differential* main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ Takes 16-256MB modules
- ◇ 12 slots
- ◇ 32MB (2×16) minimum, 2GB maximum

Expansion

- ◇ Two slots for either GSC (*EISA formfactor*) or EISA cards
- ◇ One slot for either a PCI 32-bit/33MHz, 3V or EISA card
- ◇ One slot for a PCI 32-bit/33MHz, 3V card
- ◇ Slot layout (from top to bottom):
 1. EISA or GSC
 2. EISA or GSC
 3. PCI-32/33 3V or EISA
 4. PCI-32/33

Drives

The disk-slider can accommodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- ◇ Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- ◇ One 3.5" Floppy drive and
- ◇ One external-accessible half-height 5.25" SCSI drive (CD/DAT).

4.20.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- ◇ Two DB9 male RS232C serial (up 460.8Kb/s)
- ◇ DB25 female parallel
- ◇ TP/RJ45 10Mbit Ethernet
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ EVC graphics port (*See Note 1*)
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.20.4 ROM update

There is a firmware update available for the C160L, which contains the latest version (5.8).

- ◇ PF_CB1X0058.txt⁸⁰ has details about the contents and installation of the patch.
- ◇ PF_CB1X0058⁸¹ contains the patch.

4.20.5 References

Manuals

- ◇ C160L Owners Guide⁸² (PDF, 1.6MB)
- ◇ C-Class Service handbook⁸³ (PDF, 1.6MB)

⁸⁰ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CB1X0058.txt

⁸¹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CB1X0058

⁸² <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37959/lpv37959.pdf>

⁸³ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37954/lpv37954.pdf>

- ◇ C100, C110 to C160L CPU upgrade⁸⁴ (PDF, 0.5MB)

4.20.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs very nice.
 - 11.00 and 11i: runs nicely.
- ◇ Linux: works fine.
- ◇ OpenBSD: works fine (the 53C720 Fast-Wide HVD SCSI controller is supported since release 4.2).
- ◇ NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI controller is not supported.

4.20.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
C132L	6.45	6.70	58.1	60.3
C160L	7.75	7.56	7.75/7.56	69.7/68.1

4.20.8 Physical dimensions/Power

- ◇ 138×539×447 mm height/width/depth
- ◇ 16.7kg net weight, 21.1kg fully loaded
- ◇ 525W max. power input
- ◇ 5.0A max. RMS at 240V
- ◇ 9.5A max. RMS at 120V

⁸⁴ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37952/lpv37952.pdf>

4.21 HP Visualize C160 & C180

4.21.1 Overview

The C180 is also sometimes referred to as C180XP

These were graphics workstations equipped with the 64-bit PA-8000 processor. The case is similar to that of the HP 9000/735 workstation, built of interlocking modules. These machines were aimed at CAD/CAM/3D modelling.

Model numbers: both the C160 and C180 have the HP 9000/780 model number.

4.21.2 Internals

CPU

- ◇ C160: PA-8000 160MHz with 512/512KB off-chip I/D L1 cache
 - 128-bit wide bus to cache
 - 2.56GB/s I-fetch
 - 2.56GB/s D-load (16-Byte), 1.26GB/s D-store (8-Byte)
- ◇ C180: PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache
 - 128-bit wide bus to cache
 - 2.88GB/s I-fetch
 - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ UTurn I/O adapter Runway to GSC bridge
- ◇ MMC/SMC memory controllers
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP HIL interface
- ◇ Dino GSC-to-PCI bridge

- ◇ Visualize-EG graphics
- ◇ Intel 82C503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2

Buses

- ◇ Runway CPU/memory bus (120MHz with 960MB/s peak bandwidth)
- ◇ GSC-2 general system-level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ 960MB/s peak bandwidth
- ◇ Takes 16-256MB modules (needs latest firmware-revision for large modules)
- ◇ 12 slots
- ◇ 32MB (2×16) minimum, 3GB (12×256) maximum

Expansion

- ◇ One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 3.3V card
- ◇ One slot for either a GSC (*EISA formfactor*), EISA or PCI 32-bit/33MHz, 3.3V card
- ◇ Two slots for either GSC (*EISA formfactor*) or EISA cards
- ◇ I/O slot layout (from top to bottom):
 1. EISA or GSC
 2. EISA or GSC
 3. PCI-32/33, 3.3V or EISA or GSC
 4. PCI-32/33, 3.3V or GSC

Drives

The disk-slider can accommodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- ✧ Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- ✧ One 3.5" Floppy drive and
- ✧ One external-accessible half-height 5.25" SCSI drive (CD/DAT).

4.21.3 External connectors

- ✧ 50-pin HD SCSI-2 single-ended
- ✧ 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- ✧ Two DB9 male RS232C serial (up 460.8Kb/s)
- ✧ DB25 female parallel
- ✧ TP/RJ45 10Mbit Ethernet
- ✧ 15-pin AUI 10Mbit Ethernet
- ✧ EVC graphics port (*See Note 1*)
- ✧ Two PS/2 connectors for keyboard and mouse
- ✧ HP-HIL for input device loop
- ✧ Four phone jacks (microphone, headphones, line-in and ?)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.21.4 ROM update

There is a firmware update available for the C160 and C180, which contains the latest version (6.2).

- ✧ `PF_CC2X0062.text`⁸⁵ has details about the contents and installation of the patch.

⁸⁵ [ftp://ftp.parisc-linux.org/kernels/c200/CC2X0062.text](http://ftp.parisc-linux.org/kernels/c200/CC2X0062.text)

- ◇ PF_CC2X0062.frm⁸⁶ contains the patch.

4.21.5 Operating systems

- ◇ HP-UX: every release from 10.20-11.11 works.
 - 10.20: runs very nice.
 - 11.00 and 11i: run also very nicely in either 32 or 64-bit mode.
You need EP9808 to run a 64-bit 11.0 environment on a machine with a 64-bit PA-8000.
- ◇ Linux: works fine.
- ◇ OpenBSD: runs fine (in 32-bit mode).

4.21.6 References

Manuals

- ◇ C-Class Owners Guide⁸⁷ (PDF, 1.5MB)
- ◇ C100, C110 to C160, C180 CPU upgrade⁸⁸ (PDF, 0.5MB)
- ◇ C160 to C180 CPU upgrade⁸⁹ (PDF, 0.2MB)
- ◇ C100, C110, C160, C180 to C200 CPU upgrade⁹⁰ (PDF, 0.5MB)

4.21.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
C160	10.40	16.30	93.6	147
C180	11.80	18.70	107	169

4.21.8 Physical dimensions/Power

- ◇ 138×539×447 mm height/width/depth
- ◇ 16.7kg net weight, 21.1kg fully loaded
- ◇ 525W max. power input
- ◇ 5.0A max. RMS at 240V
- ◇ 9.5A max. RMS at 120V

⁸⁶ <ftp://ftp.parisc-linux.org/kernels/c200/CC2X0062.frm>

⁸⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37673/lpv37673.pdf>

⁸⁸ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37949/lpv37949.pdf>

⁸⁹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37957/lpv37957.pdf>

⁹⁰ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf>

4.22 HP Visualize C200, C240 & C360

4.22.1 Overview

Sometimes referred to as C200+ and C240+

These were aimed at the graphics workstations market, equipped with the 64-bit PA-8200 and PA-8500 CPUs. They have a similar case to that of the old 735 — built of interlocking modules so the I/O board, MPU board etc. can be easily taken out. These machines were aimed at CAD/CAM/3D modelling.

Model numbers:

- ◇ C200, C240: 9000/782
- ◇ C360: 9000/785

4.22.2 Internals

CPU

- ◇ C200: PA-8200 200MHz with 512/1024KB off-chip I/D L1 cache
- ◇ C240: PA-8200 236MHz with 2048/2048KB off-chip I/D L1 cache
- ◇ C360: PA-8500 367MHz with 512/1024KB on-chip I/D L1 cache

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ UTurn I/O adapter Runway to GSC bridge
- ◇ MMC/SMC memory controllers
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
- ◇ Dino GSC-to-PCI bridge
- ◇ Cujo GSC-to-PCI bridge
- ◇ Intel 82C503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller

- ◇ Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- ◇ DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- ◇ Runway CPU/memory bus (120MHz with 960MB/s peak data rate)
- ◇ GSC-2 general system-level I/O bus
- ◇ EISA (built to order option), additional expansion I/O
- ◇ PCI-32/33 device I/O bus
- ◇ PCI-64/66 high-performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ SCSI-2 Ultra-Wide single-ended bus main storage I/O

Memory

- ◇ 72-pin ECC EDO SIMMs, 50ns or faster (should run with 60ns modules too)
- ◇ Takes 16-256MB modules (needs latest firmware-rev)
- ◇ 12 slots
- ◇ 32MB (2×16) minimum, 3GB (12×256) maximum

Expansion

- ◇ Three slots for either GSC (*EISA formfactor*) or PCI cards
- ◇ One slot for either a GSC (*EISA formfactor*), PCI or EISA card
- ◇ Two of the PCI slots are PCI 32-bit/33MHz, 5V; the other two PCI 64-bit/66MHz, 3.3V.
Some system do not have the optional EISA slot
- ◇ I/O slot layout (from top to bottom):
 1. PCI-32/33, 5V or EISA or GSC
 2. PCI-64/66, 3.3V or GSC
 3. PCI-32/33, 5V or GSC
 4. PCI-64/66, 3.3V or GSC

Drives

The disk-slider can accommodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a SE-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily

replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Ultra-Wide SE system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Ultra-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- ✧ Two 3.5" 68-pin Ultra-Wide single-ended (SE) SCSI hard drives,
- ✧ One 3.5" Floppy drive and
- ✧ One external-accessible half-height 5.25" SCSI drive (CD/DAT).

4.22.3 External connectors

- ✧ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ✧ 68-pin HD SCSI-3 Ultra-Wide single-ended
- ✧ Two DB9 male RS232C serial
- ✧ DB25 female parallel
- ✧ TP/RJ45 10/100Mbit Ethernet
- ✧ 15-pin AUI 10Mbit Ethernet
- ✧ Two PS/2 connectors for keyboard & mouse
- ✧ Four phone jacks (microphone, headphones, line-in and ?)

4.22.4 ROM update

There is an firmware update available for the C200 & C240, which contains the latest version (6.3).

- ✧ `PF_CC2X0063.txt`⁹¹ has details about the contents and installation of the patch.
- ✧ `PF_CC2X0063`⁹² contains the patch.

There is also an firmware update available for the C360, which contains the latest version (1.5).

- ✧ `PF_CC360015.txt`⁹³ has details about the contents and installation of the patch.
- ✧ `PF_CC360015`⁹⁴ contains the patch.

4.22.5 References

Manuals

- ✧ **C-Class Owners Guide**⁹⁵ (PDF, 1.5MB)

⁹¹ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC2X0063.txt

⁹² ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC2X0063

⁹³ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC360015.txt

⁹⁴ ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC360015

⁹⁵ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37673/lpv37673.pdf>

- ◇ C-Class Service handbook⁹⁶ (PDF, 1.6MB)
- ◇ C100, C110, C160, C180 to C200 CPU upgrade⁹⁷ (PDF, 0.5MB)
- ◇ C200 to C240 CPU upgrade⁹⁸ (PDF, 0.2MB)
- ◇ C200, C240 to C360 CPU upgrade⁹⁹ (PDF, 0.2MB)

Other

- ◇ HP C200/C240/C360 Power Supply problems - solved¹⁰⁰ USENET posting

4.22.6 Operating systems

- ◇ HP-UX: every release from 10.20 *ACE 9707* - 11.11 works.
 - 10.20: very fast
You need at least *ACE 9707*.
 - 11.00 and 11i: run nicely. You need *EP9808* to run a 64-bit 11.0 environment
- ◇ Linux: works fine.
- ◇ OpenBSD: runs fine (in 32-bit mode).

4.22.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
C200	14.20	21.40	129	193
C240	17.10	25.40	156	229
C360	26.00	28.10	234	252

4.22.8 Physical dimensions/Power

- ◇ 138×539×447mm height/width/depth
- ◇ 17.7kg net weight, 22.7kg fully loaded
- ◇ 880W max. power input
- ◇ 5A max. RMS at 240V
- ◇ 10A max. RMS at 120V

⁹⁶ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37954/lpv37954.pdf>

⁹⁷ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf>

⁹⁸ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37960/lpv37960.pdf>

⁹⁹ <http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37961/lpv37961.pdf>

¹⁰⁰ <http://groups.google.de/groups?selm=20041127170355.H89099@calchas.unixiron.org>

4.23 HP Visualize B1000, C3000 & C3600

4.23.1 Overview

These workstations were aimed at the graphics workstations market, equipped with the 64-bit PA-8500 featuring large on-chip L1 caches. The C3600 is essentially a C3000 upgraded to a PA-8600 CPU, the C3700 is the same, but upgraded to a PA-8700 CPU. There were additionally various more upgraded models, *e.g.*, the C3650 and the C3750, the former with a faster PA-8700 CPU, the latter with an even faster PA-8700+ CPU. The architecture was a major change from those of its predecessors, *e.g.*, the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports. The case also was a major redesign.

Model numbers:

- ✧ B1000 and all C3x00/C3x50 have the 9000/785 model number

4.23.2 Internals

CPU

- ✧ B1000: PA-8500 300MHz with 512/1024KB on-chip I/D L1 cache
- ✧ C3000: PA-8500 400MHz with 512/1024KB on-chip I/D L1 cache
- ✧ C3600: PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache
- ✧ C3650: PA-8700 625MHz with 768/1536KB on-chip I/D L1 cache
- ✧ C3700: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache
- ✧ C3750: PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache

Chipset

- ✧ Astro memory/Runway controller
- ✧ Four Elroy PCI bridges
- ✧ National 87560 (*SuperI/O*), handling USB, RS232, parallel, floppy and IDE
- ✧ National 87415 IDE controller
- ✧ National USB controller
- ✧ Analog Devices AD1889 sound chip
- ✧ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ✧ Symbios Logic 53C896 SCSI-3 controller

Buses

- ✧ Runway CPU/memory bus

- ◇ PCI-32/33 device I/O bus
- ◇ PCI-64/33 high-performance device I/O bus
- ◇ PCI-64/66 high-performance graphics I/O bus
- ◇ C37x0: PCI-64/100 high-performance graphics I/O bus
- ◇ SCSI-2 Ultra-Narrow single-ended external I/O bus
- ◇ SCSI-3 Ultra2-Wide LVD storage I/O bus
- ◇ IDE removable device I/O bus (can partially boot from CD-ROM, *e.g.*, HP-UX)

Memory

- ◇ 278-pin 120MHz ECC SDRAM DIMMs
- ◇ Takes 128/256/512/1024MB modules (needs latest firmware revision)
- ◇ Eight slots
- ◇ 128MB (1×128) minimum, 8GB (8×1GB) maximum

Expansion

- ◇ One PCI 64-bit/66MHz, 3.3V slot (clocked at 100MHz on C37x0 systems)
- ◇ Three PCI 64-bit/33MHz, 5V slots
- ◇ Two PCI 32-bit/33MHz, 5V slots
- ◇ I/O slot layout (from top to bottom):
 1. PCI-64/33, pcio, 5V
 2. PCI-64/66, pci1, 3.3V (for primary graphics) [on C37x0 systems this is a PCI-64/100 slot]
 3. PCI-64/33, pcio, 5V
 4. PCI-64/33, pci2, 5V (for secondary graphics)
 5. PCI-32/33, pci3, 5V
 6. PCI-32/33, pci3, 5V

Drives

- ◇ One tray for two 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector
- ◇ One tray for a 3.5" Floppy drive
- ◇ One tray for a half-height 5.25" IDE drive, external accessible

4.23.3 External connectors

- ◇ 50-pin HD SCSI-2 Ultra-Narrow single-ended
- ◇ 68-pin HD SCSI-3 Ultra2-Wide LVD
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ Two USB ports for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

4.23.4 ROM update

There is a firmware update available for the **PA-8500 and PA-8600**-based B1000, C3000 and C3600 which contains the latest version (5.0).

- ◇ **PF_CBCJ0050.txt**¹⁰¹ has details about the contents and installation of the patch.
- ◇ **PF_CBCJ0050**¹⁰² contains the patch.

A different firmware update is provided for the **PA-8700**-based C37x0 systems (version 2.0):

- ◇ **PF_CCJ70020.txt**¹⁰³ has details about the contents and installation of the patch.
- ◇ **PF_CCJ70020**¹⁰⁴ contains the patch.

4.23.5 References

Manuals

- ◇ **B1000/C3x00 Owner's Guide**¹⁰⁵ (PDF, 4.9MB)
- ◇ **B1000/C3x00 Service Handbook**¹⁰⁶ (PDF, 3.2MB)
- ◇ **VISUALIZE Workstation Memory Subsystem**¹⁰⁷ (PDF, 120KB)

4.23.6 Operating systems

- ◇ HP-UX:
 - B1000, C3000: 10.20 ACE 9906
 - C3600: 10.20 ACE 9912

¹⁰¹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt

¹⁰²http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050

¹⁰³http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020.txt

¹⁰⁴http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020

¹⁰⁵<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37930/lpv37930.pdf>

¹⁰⁶<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37739/lpv37739.pdf>

¹⁰⁷<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf>

– 11.00 minimum *EP 9808* [not sure—*Ed.*] or *ACE9911*, and 11i v1 (both only 64-bit releases)

◇ Linux: works

◇ OpenBSD (32-bit): works

4.23.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95 <i>rate</i> , int	SPEC95 <i>rate</i> , fp	SPEC2000, int	SPEC2000, fp	SPEC2000 <i>rate</i> , int	SPEC2000 <i>rate</i> , fp
B1000	23.9	39.3	217	378				
C3000	31.8	52.4	287	471	313	321		
C3600	42.0	64.0	379	576	432	433	5.0	5.0
C3650					508	542	5.9	6.3
C3700					604	576	7.0	6.7
C3750					678	674		

4.23.8 Physical dimensions/Power

- ◇ 445×229×495 mm height/width/depth
- ◇ rack-mounted: 6U height, 451×665 mm width/depth
- ◇ 20.9kg net weight, 25.4kg fully loaded
- ◇ 805W max power input
- ◇ 3.8A max RMS at 240V
- ◇ 7.4A max RMS at 120V

4.24 HP C8000

4.24.1 Overview

The c8000 is the latest and probably last PA-RISC HP workstation. It is driven by one or two dual-core PA-8800 *Mako* processors, later offered with PA-8900 CPUs and features an impressive array of system and I/O options. The center of the system is the HP *zx1* chipset, which also supports Itanium processors. The system is built in a sleek, silent tower casing and also available as a rack-mount option.

Time of introduction: 2004

4.24.2 Internals

CPU

- ◇ 1-2 PA-8800 (dual-core) 900MHz-1.0GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each
- or
- ◇ 1-2 PA-8900 (dual-core) 800MHz-1.1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 64MB off-chip L2 cache each

Chipset

- ◇ HP *zx1* chipset
 - *zx1* MIO (memory and I/O controller) connects to the processor bus (6.4GB/s), two memory buses (each 4.25GB/s) and seven I/O channels (aggregate 3.5GB/s) and contains both memory and cache controllers
 - Six *zx1* IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the *zx1* MIO with an aggregate bandwidth of 3.5GB/s on seven 0.5GB/s channels
 1. AGP 4x graphics bus on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 3. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 4. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 5. Gigabit Ethernet and Ultra320 SCSI on PCI 64/66 on one channel — 0.5GB/s
 6. IDE, USB, management LAN on PCI 32/33 on one channel — 0.5GB/s
- ◇ Gigabit Ethernet controller
- ◇ Two-channel Ultra-320 SCSI controller
- ◇ UltraATA-133 IDE controller
- ◇ 8MB Flash EEPROM

The detailed layout of the zx1 chipset and I/O adapters (IOAs) is approximate — no system-level descriptions were found and the information inferred from bus layout.

Buses

- ◇ Itanium 2/ZXI processor bus 6.4GB/s
- ◇ Two independent ZXI memory buses, 266MHz, each 4.25GB/s—aggregate 8.5GB/s memory bandwidth
- ◇ Seven ZXI I/O channels/buses, aggregate 3.5GB/s
- ◇ AGP 8x graphics bus
- ◇ PCI-X 64/133 I/O bus
- ◇ PCI-X 64/66 I/O bus
- ◇ PCI 64/33 I/O bus
- ◇ PCI 32/33 I/O bus
- ◇ SCSI-3 Ultra320 (LVD) storage I/O bus
- ◇ UltraATA-133 IDE secondary storage I/O bus

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Takes up to 4GB modules
- ◇ Eight slots
- ◇ 32GB maximum
- ◇ 8.5GB/s memory bandwidth
- ◇ 8ns memory latency

Expansion

- ◇ One PCI-X 64-bit/133MHz slot, full-length
- ◇ Two PCI-X 64-bit/66MHz slots, full-length
- ◇ One PCI 64-bit/33MHz slot, full-length
- ◇ Two PCI 32-bit/33MHz slots, half-length
- ◇ All PCI slots are 3.3V
- ◇ One AGP Pro 8x slot (150W max power with auxiliary power connector)
- ◇ I/O slot layout (from top to bottom):
 1. PCI-32/33, short PCI cards
 2. PCI-32/33, short PCI cards
 3. AGP-8X pro
 4. PCI-64/33, short and full-length cards

5. PCI-64/66, short and full-length cards
6. PCI-64/66, short and full-length cards
7. PCI-64/133, short and full-length cards

Drives

- ◇ Up to four internal 3.5" bays for Ultra320 LVD SCSI hard drives with 68-pin connector
- ◇ Up to two internal 3.5" bays for UltraATA-133 IDE hard drives
- ◇ Three half-height 5.25" bays for externally accessible SCSI (LVD or SE) or UltraATA-133 drives

4.24.3 External connectors

- ◇ Two DB9 male RS232C serial
- ◇ Five USB 2.0 ports (two in front, three in rear)
- ◇ TP/RJ45 Gigabit Ethernet
- ◇ Four phone jacks (microphone, headphones, line-in and line-out) on optional 16-bit audio card

4.24.4 ROM update

There is an firmware update available which contains the latest version 2.13.

- ◇ PF_CC8K0213.txt¹⁰⁸ has details about the contents and installation of the patch.
- ◇ PF_CC8K0213¹⁰⁹ contains the patch.

4.24.5 References

Manuals

- ◇ HP Workstation c8000 Technical Reference Guide¹¹⁰ (PDF, 2.7MB)

Articles

- ◇ HP c8000 data sheet¹¹¹ (PDF, 400KB)

4.24.6 Operating systems

- ◇ HP-UX: 11i v1 TCOE and MTOE

¹⁰⁸http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC8K0213.txt

¹⁰⁹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC8K0213

¹¹⁰<http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00093136/c00093136.pdf>

¹¹¹<http://www.hp.com/workstations/risc/c8000/c8000.pdf>

4.24.7 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
C8000		1001 (est.)		

4.24.8 Physical dimensions/Power

- ◇ 490×287×572 mm height/width/depth
- ◇ Rack-mounted: 5U height, 424×572 mm width/depth
- ◇ 18.6kg net weight, 21.4kg fully loaded
- ◇ 871W max. power input (410W typical “workstation configuration”)

4.25 HP 9000/D-Class & R-Class

4.25.1 Overview

The D-Class *Ultralight* were designed to be flexible, upgradable and scalable Enterprise servers. Many different models were sold which could be upgraded within the series to another model with various options for each system. They were designated to bring “mid-range performance for an entry-level price.” Some are two-way SMP capable, supported CPUs range from 32-bit PA-7100LC to 64-bit PA-8200.

The R-Class *Ultralight* servers (R380/R390) are the rack-mountable versions of their D-Class counterparts (D380/D390). They are technically almost identical, except some differences in the I/O and storage configuration.

The Ultralight servers used the following naming convention:

- ◇ The first number after the “D”, — 2 or 3 — indicates the general type — D-Class servers were available in two different versions: the smaller D2x0 and the bigger D3x0.
- ◇ The latter numbers [00, 10, ..., 90] indicate the “internal” features, like CPU and chipset.
- ◇ The R-Class R380/R390 are D380/D390 in a rack-mountable (19”) case.

Model numbers and introductions dates:

System	Model number	Introduced	Price
D200, D300	HP 9000/801	January 1996	
D210, D310	HP 9000/811	January 1996	\$6,900, ?
D220, D320	HP 9000/803, HP 9000/813	January 1997	\$8,900, ?
D230, D330	HP 9000/823, HP 9000/833	January 1997	?, \$16,700
D250, D350	HP 9000/821, HP 9000/831	January 1996	
D260, D360	HP 9000/841, HP 9000/851	May 1996	
D270, D370	HP 9000/861, HP 9000/871	November 1996	
D280, D380	HP 9000/810, HP 9000/820	September 1997	
D390	HP 9000/800	July 1998	
R380, R390	HP 9000/800	September 1998	

4.25.2 Internals

CPU

- ◇ D200: PA-7100LC 75MHz with 1KB on-chip I L1 and 256KB off-chip unified L1 cache
- ◇ D210: PA-7100LC 100MHz with 1KB on-chip I L1 and 256KB off-chip unified L1 cache
- ◇ D220: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- ◇ D230: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- ◇ D250: 1-2 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache each
- ◇ D260: 1-2 PA-7200 120MHz with 1024/1024KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache each

- ◇ Dx70: 1-2 PA-8000 160MHz with 512/512KB off-chip I/D L1 cache each
- ◇ Dx80/R380: 1-2 PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache each
- ◇ D390/R390: 1-2 PA-8200 240MHz with 2048/2048KB off-chip I/D L1 cache each

Notes

- ◇ Systems with PA-7100LC/PA-7300LC processors are not SMP capable
- ◇ The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache
- ◇ The 2KB on-chip “assist” cache on systems with a PA-7200 is not really a true cache
- ◇ Systems with a PA-7300LC processor feature an optional 1MB external L2 cache, provided through two SRAM modules
- ◇ Upgrading from one type of CPU to another mostly requires more than just changing the CPU board (cf. *D-Class and R-Class System Upgrade Guide*).

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit audio
 - NS 16550A compatible serial
- ◇ PA-7200 models: U2 I/O adapter Runway to GSC bridge
- ◇ PA-8000 models: UTurn I/O adapter Runway to GSC bridge
- ◇ PA-7200/PA-8000 models: MMC/SMC memory controllers
- ◇ PA-7300LC models: Phantom PseudoBC GSC+ port
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ D3x0: NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- ◇ D390/R380/R390: DEC 21140 Fast Ethernet controller

Buses

- ◇ On SMP-capable systems: Runway CPU/memory bus

- ◇ GSC+ bus for the general system level I/O
- ◇ EISA expansion bus
- ◇ D3x0: SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- ◇ SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Note: the Fast-Wide differential bus is optional on the D2x0 models.

Memory

- ◇ 72-pin ECC SIMMs

The required access-time of the RAM modules depends on the used CPU, systems with a PA-8x00 will need 50ns modules, those with PA-7200 and PA-7300LC can take up to 60ns and PA-7100LC-based models can take even slower modules.

Expansion

- ◇ D2x0:
 - One slot for a GSC/HSC (EISA formfactor) card
 - Two slots for EISA cards
 - Three slots for either GSC/HSC (EISA formfactor) or EISA cards
- ◇ D3x0:
 - One slot for a GSC/HSC (EISA formfactor) card
 - Three slot for EISA cards
 - Four slots for either GSC/HSC (EISA formfactor) or EISA cards
- ◇ R380/R390:
 - One slot for a GSC/HSC (EISA formfactor) card
 - Four slot for EISA cards
 - Three slots for either GSC/HSC (EISA formfactor) or EISA cards

Drives

- ◇ D2x0/R3x0: Up to two Fast-Narrow 50-pin SCSI-2 single-ended hard drives
- ◇ D3x0: five hot-swap trays for a Fast-Wide 68-pin SCSI-2 high-voltage differential hard drive
- ◇ D-Class: Up to three 5.25" 50-pin Fast-Narrow SE SCSI half-height drives, external accessible
- ◇ R3x0: On 5.25" 50-pin Fast-Narrow SE SCSI half-height drive, external accessible

Note: If the Fast-Wide differential SCSI option exists on a D2x0, two optional trays for FWD drives are available.

4.25.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ TP/RJ45 10BaseT 10Mbit Ethernet
- ◇ Two DB9 male RS232C serial, one for console, one for USV
- ◇ DB25 female parallel
- ◇ Two PS/2 connectors for keyboard und mouse

4.25.4 ROM update

There is a firmware update available for the D210 and D310 which contains the latest version (38.43).

- ◇ PF_CULL3843.txt¹¹² has details about the contents and installation of the patch.
- ◇ PF_CULL3843¹¹³ contains the patch.

There is also a firmware update available for the D220, D230, D320 and D310 which contains the latest version (38.46).

- ◇ PF_CULD3846.txt¹¹⁴ has details about the contents and installation of the patch.
- ◇ PF_CULD3846¹¹⁵ contains the patch.

There is also a firmware update available for the D250, D260, D350 and D360 which contains the latest version (36.34).

- ◇ PF_CULT3634.txt¹¹⁶ has details about the contents and installation of the patch.
- ◇ PF_CULT3634¹¹⁷ contains the patch.

There is also a firmware update available for the D270, D280, D370, D380 and R380 which contains the latest version (42.11).

- ◇ PF_CULU4211.txt¹¹⁸ has details about the contents and installation of the patch.
- ◇ PF_CULU4211.frm¹¹⁹ contains the patch.

There is also a firmware update available for the D390 and R390 which contains the latest version (42.10).

- ◇ PF_CULV4210.txt¹²⁰ has details about the contents and installation of the patch.
- ◇ PF_CULV4210.frm¹²¹ contains the patch.

¹¹²http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULL3843.txt

¹¹³http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULL3843

¹¹⁴http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULD3846.txt

¹¹⁵http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULD3846

¹¹⁶http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULT3634.txt

¹¹⁷http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULT3634

¹¹⁸http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULU4211.txt

¹¹⁹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULU4211.frm

¹²⁰http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULV4210.txt

¹²¹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULV4210.frm

4.25.5 References:

Manuals

- ◇ D-Class and R-Class Installation Guide¹²² (PDF, 0.4MB)
- ◇ D-Class and R-Class Operator's Guide¹²³ (PDF, 1.1MB)
- ◇ D-Class and R-Class System Upgrade Guide¹²⁴ (PDF, 0.9MB)

Articles

- ◇ An Entry-Level Server with Multiple Performance Points¹²⁵ (.pdf) Lin A. Nease et al (June 1997: Hewlett-Packard Journal)

4.25.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works. Systems with a 64-bit PA-800 CPU also can use 64-bit version of HP-UX 11.x.
 - 10.20 for 800s servers: runs nicely.
 - 11.00 and 11.11 vi: run nicely.
- ◇ Linux: works.
- ◇ D220/230, D320/330: OpenBSD works.

4.25.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
Dx00	115	146	2.18	2.90	19.2	25.8
Dx10	152	194	3.74	4.08	33.6	36.7
Dx20			6.57	6.72	59.2	60.5
Dx30			7.87	7.58	70.8	68.3
Dx50	144	218	5.01	6.77	45.1	61.0
Dx60						
Dx60					114	143
Dx70			10.40	15.00	93.9	135
Dx702-CPU					184	190
Dx80			12.30	17.40	111	157
Dx802-CPU					219	221
D390			15.50	25.50		

¹²²<http://docs.hp.com/hpux/pdf/A3262-90057.pdf>

¹²³<http://docs.hp.com/hpux/pdf/A3262-90013.pdf>

¹²⁴<http://docs.hp.com/hpux/pdf/A3262-90010.pdf>

¹²⁵<http://www.hpl.hp.com/hpjournal/97jun/jun97a10.pdf>

4.26 HP 9000/E-Class

4.26.1 Overview

The E-Class “Wright Brothers” are low-cost PA-RISC servers from the mid-1990s and the replacements for the older F and G-Class Nova servers. Designed for reduced manufacturing cost they were developed in parallel to the HP 9000/712 workstations. The case was taken over almost unchanged from the F-Class, with the CPU/memory and part of the I/O systems being new designs. From the integrated LASI chipset only the networking and several other functions were used — due to time constraints a modified version of the F-Class HP-PB “Personality boards” was used for SCSI, serial MUX and parallel.

Model numbers, introductions dates and prices:

System	Model number	Introduced	Price
E25	HP 9000/806	1994	\$6,000
E35	HP 9000/816	1994	
E45	HP 9000/826	1994	\$11,320
E55	HP 9000/856	1995?	

4.26.2 Internals

CPU

- ✧ E25: PA-7100LC 48MHz with 1KB on-chip I L1 and 64KB off-chip unified I/D L1 cache
- ✧ E35: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ✧ E45: PA-7100LC 80MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- ✧ E55: PA-7100LC 96MHz with 1KB on-chip I L1 and 1024KB off-chip unified I/D L1 cache

Notes

1. The 1KB on-chip L1 cache is not really a true cache.

Chipset

- ✧ LASI as central I/O chipset (not all functions are used)
- ✧ Wax ASIC
- ✧ HP-PB bus converter
 - 8MHz HP-PB frequency
 - Implemented from the HP_PB converter of the old HP 9000 F and G servers
 - GSC to HP-PB clock ratio from 3:1 to 5:1 synchronous with 32MHz GSC frequency
 - GSC to HP-PB clock ratio asynchronous with GSC frequency between 32 to 40MHz
 - 0.8µin 208-pin MQFP
- ✧ Several HP ASICs, controlling the HP-PB SCSI and MUX port

Buses

- ◇ GSC system level I/O bus (128MB/s)
- ◇ HP-PB additional I/O bus (32MB/s)
- ◇ SCSI-2 Fast-Narrow single-ended bus; main storage I/O

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-64MB modules
- ◇ Eight slots
- ◇ 16MB (2×8) minimum, 512MB (8×64) maximum

Expansion

- ◇ Two slots for HP-PB cards

Drives

- ◇ One tray for two 3.5" Fast-Narrow SE 50-pin SCSI hard drives
- ◇ One tray for three half-height 5.25" Fast-Narrow SE 50-pin drives, externally accessible

4.26.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ high-pin-count MUX connector
- ◇ TP/RJ45 10Mbit Ethernet (*See Note 1*)
- ◇ 15-pin AUI 10Mbit Ethernet (*See Note 1*)
- ◇ DB25 female parallel

Notes

1. The system automatically detects the used port.

4.26.4 ROM update

There is a firmware update available for the E25, E35 and E45, which contains the latest version (1.3).

- ◇ PF_CWBR0013.txt¹²⁶ has details about the contents and installation of the patch.
- ◇ PF_CWBR0013¹²⁷ contains the patch.

¹²⁶[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013.txt](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013.txt)

¹²⁷[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013)

4.26.5 References

Articles

- ◇ Development of a Low-Cost, High-Performance, Multiuser Business Server System¹²⁸ (PDF, HP Journal 4/95)
- ◇ HP 9000 E-Class Servers Product Brief¹²⁹ (.pdf) Hewlett-Packard Company (1993: Hewlett-Packard)

4.26.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.00 works.
 - 10.20 for 800s servers: runs nicely.
 - 11.00: runs nicely.
 - 11i: officially unsupported but some releases work. Faster than 11.00 on the same hardware.
- ◇ Linux: works, but the hardware support for the E-class is very limited, *i.e.*, the SCSI subsystem does not work.
- ◇ NetBSD: experimental support as of 5/2005, however some I/O devices are not supported (*e.g.*, SCSI).

4.26.7 Benchmarks

Model	SPEC92, int	SPEC92, fp
E25	45.0	66.7
E35	65.6	98.5
E45	82.1	122.9
E55	108.0	163.4

¹²⁸<http://www.hpl.hp.com/hpjournal/95apr/apr95a10.pdf>

¹²⁹<http://www.hpmuseum.net/document.php?hwfile=3745>

4.27 HP 9000 Series 800 Nova Servers

4.27.1 Overview

The *Nova* servers are second-generation 32-bit HP 9000/800 PA-RISC servers, released in the early 1990s and based on the PA-7000 and PA-7100 processors. They were available in different sizes with different expansion options, CPUs and clock speeds.

The Nova servers have the following naming convention:

- ◇ The first letter [F, G, H, I] indicates the “external” features, like casing and expansion
- ◇ The number [10, 20, ..., 70] indicates the “internal” features, like CPU and chipset

They were succeeded in the HP 9000/800 series by the PA-7100LC E-Class servers which have a similar case as the F-Class.

Introduced: 1991-1993

Model numbers and prices at introduction:

System	Model number	Price
F10	HP 9000/807	
F20, H20	HP 9000/817, HP 9000/827	
F30, G30/H30, I30	HP 9000/837, HP 9000/847, HP 9000/857	
G40/H40, I40	HP 9000/867, HP 9000/877	G40: \$112,500, I40: \$140,000
G50/H50, I50	HP 9000/887, HP 9000/897	
G60/H60, I60	HP 9000/887, HP 9000/897	
G70/H70, I70	HP 9000/887, HP 9000/897	

4.27.2 Internals

CPU

- ◇ F10: PA-7000 32MHz with 32/64KB off-chip I/D L1 cache
- ◇ x20: PA-7000 48MHz with 64/64KB off-chip I/D L1 cache
- ◇ x30: PA-7000 48MHz with 256/256KB off-chip I/D L1 cache
- ◇ x40: PA-7000 64MHz with 256/256KB off-chip I/D L1 cache
- ◇ x50: PA-7100 96MHz with 256/256KB off-chip I/D L1 cache
- ◇ x60: PA-7100 96MHz with 1024/1024KB off-chip I/D L1 cache
- ◇ x70: 1-2 PA-7100 96MHz with 2048/2048KB off-chip I/D L1 cache each

On systems with PA-7000 processors the FPU was optional — there is often an empty socket on the processor board.

Chipset

The chipset is based on a variant of the ASP chipset, with at least the Viper memory controller interfacing the processor to memory and the HP-PB I/O bus. The rest of the system I/O is implemented on so-called HP-PB “Personality Boards.”

Buses

- ◇ PBus processor/memory bus (64MHz on I70: 256MB/s)
- ◇ VSC main system bus
- ◇ HP-PB bus for the general I/O
- ◇ SCSI-2 Narrow single-ended bus for main storage I/O

Memory

- ◇ HP proprietary modules (same as those on 720, 730 and 750, and 735/755)
- ◇ 12 slots
- ◇ F10: 16MB minimum, 128MB (8×16MB) maximum
- ◇ F20 and F30: 16MB minimum, 192MB (12×16MB) maximum
- ◇ H20, H30, G30, I30, x40: 16MB minimum, 384MB (12×32MB) maximum
- ◇ x50, x60, x70: 16MB minimum, 768MB (12×64MB) maximum

Expansion

- ◇ Fx0: two HP-PB single-height/one double-height
- ◇ Gx0: six HP-PB single-height/three double-height
- ◇ Hx0: six HP-PB single-height/three double-height
- ◇ Ix0: 12 HP-PB single-height/six double-height

Drives

- ◇ ? (many)

4.27.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ High-pin-count MUX connector
- ◇ DB25 female parallel
- ◇ Rest depends on installed HP-PB cards

4.27.4 References

Manuals

- ◇ **Owner's Guide to the HP 9000 8x7S Family**¹³⁰ (.pdf) Hewlett-Packard Company (1991. Accessed January 2009 at hpmuseum.net)
- ◇ **CE Handbook Series 9x7 and Model 8x7S Family**¹³¹ (.pdf) Hewlett-Packard Company (February 1992, edition E0292, part number A1707-90016. Accessed January 2009 at hpmuseum.net)

Other

- ◇ Pinout for the mini-DIN console connector at the back

4.27.5 Operating systems

The only operating system that runs on these servers is HP-UX—all of these servers are officially supported in versions 10.20 for 800s servers and 11.00. (The first supported release was HP-UX 8.02.) Official support for the Nova servers was dropped in 11.11 (11i), however it is still possible in most cases to install and run 11i on these systems.

It is unlikely if there will ever be a port of an “open” operating system, as not much documentation exist on the I/O and system details.

4.27.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	MIPS
F10	22.0	36.6	35
x20	33.6	56.1	53
x30	37.8	62.4	53
x40	65.2	91.3	70
x50	100.0	158.5	115
x60	108.8	195.3	115
x70	108.8	195.3	115

All results are for single-CPU systems.

¹³⁰<http://www.hpmuseum.net/document.php?hwfile=3246>

¹³¹<http://www.hpmuseum.net/document.php?hwfile=2653>

4.28 HP Visualize J200, J210, J280 & J2240

4.28.1 Overview

The J-Class are SMP-capable and expandable PA-RISC workstations. They feature a deskside chassis with four interlocked modules, which you can take out easily for maintenance. The J280 is only a single-processor machine, which can be upgraded to a dual-capable J282. This requires at least changing the mainboard.

Model numbers:

- ◇ J200, J210, J210XC: HP 9000/770
- ◇ J280, J282: HP 9000/780
- ◇ J2240: HP 9000/782

4.28.2 Internals

CPU

- ◇ J200: 1-2 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache
 - 64-bit wide bus to cache
 - 800MB/s I-fetch (8-Byte)
 - 800MB/s D-load (16-Byte), 800MB/s single D-store (8-Byte)
- ◇ J210: 1-2 PA-7200 120MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache
 - 64-bit wide bus to cache
 - 960MB/s I-fetch (8-Byte)
 - 960MB/s D-load (16-Byte), 960MB/s single D-store (8-Byte)
- ◇ J210XC: 1-2 PA-7200 120MHz with 1/1MB off-chip I/D L1 and 2KB on-chip “assist” L1 cache
 - 64-bit wide bus to cache
 - 960MB/s I-fetch (8-Byte)
 - 960MB/s D-load (16-Byte), 960MB/s single D-store (8-Byte)
- ◇ J280: 1 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache
 - 128-bit wide bus to cache
 - 2.88GB/s I-fetch
 - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)
- ◇ J282: 1-2 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache
 - 128-bit wide bus to cache
 - 2.88GB/s I-fetch
 - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)

- ◇ J2240: 1-2 PA-8200 236MHz with 2/2MB external I/D L1 cache

The 2KB on-chip “assist” cache is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ PA-7200-models: U2 I/O adapter Runway to GSC bridge
- ◇ PA-8000/PA-8200-models: UTurn I/O adapter Runway to GSC bridge
- ◇ MMC/SMC memory controllers
- ◇ Wax chip
 - EISA bus converter (GSC-to-EISA)
 - Second RS232 serial
 - HP HIL interface
- ◇ Intel 82C503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- ◇ J2240: Dino GSC-to-PCI bridge
- ◇ J2240: Cujo GSC-to-PCI bridge
- ◇ J2240: Symbios Logic 53C895 16-bit Ultra-Wide SCSI-2 controller
- ◇ J2240: DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- ◇ Runway CPU/memory bus (100MHz with 800MB/s peak data rate on J200, 120MHz 960MB/s on all others)
- ◇ GSC system level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 Fast-Wide *high-voltage differential* bus; main storage I/O
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ J2240: SCSI-3 Ultra-Wide single-ended bus; main storage I/O
- ◇ J2240: PCI bus;

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ J200: 800MB/s peak bandwidth
- ◇ J210[XC]: 960MB/s peak bandwidth
- ◇ Take 16-128MB modules (needs latest firmware-rev)
- ◇ 16 slots
- ◇ 32MB (2×16) minimum, 2GB (16×128) maximum
- ◇ J2240: 4GB maximum (with 256MB modules)

Expansion

- ◇ One slot for a GSC (*EISA formfactor*) card
- ◇ Two slots for EISA cards
- ◇ Two slots for either GSC (*EISA formfactor*) or EISA cards
- ◇ Slot layout (from bottom to top):
 1. GSC (for primary graphics)
 2. EISA or GSC
 3. EISA or GSC
 4. EISA
 5. EISA

J2240 has different slots:

- ◇ One slot for a PCI 32-bit/33MHz, 5V card
- ◇ One slot for either a PCI 32-bit/33MHz, 5V or EISA card
- ◇ One slot for either a GSC or PCI 32-bit/33MHz, 5V card
- ◇ Two slots for either GSC or PCI 64-bit/66MHz, 3.3V cards
- ◇ Slot layout (from bottom to top):
 1. PCI-64/66, 3.3V or GSC (for primary graphics)
 2. PCI-32/33, 5V or GSC
 3. PCI-64/66, 3.3V or GSC
 4. PCI-32/33, 5V
 5. PCI-32/33, 5V or EISA

Drives

- ✧ One tray for two 3.5" Fast-Wide HVD 68-pin SCSI hard drives
- ✧ One tray for two half-height 5.25" Fast-Narrow SE 50-pin SCSI drives, external accessible

4.28.3 External connectors

- ✧ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ✧ 68-pin HD SCSI-3 Fast-Wide *high-voltage differential* (HVD)
- ✧ J2240: 68-pin HD SCSI-3 Ultra-Wide single-ended
- ✧ Two DB9 male RS232C serial (up to 460.8Kb/s)
- ✧ DB25 female parallel
- ✧ TP/RJ45 10Mbit Ethernet /
- ✧ J2240: TP/RJ45 10/100Mbit Ethernet
- ✧ 15-pin AUI 10Mbit Ethernet
- ✧ Graphics port depends on installed framebuffer
- ✧ Two PS/2 connectors for keyboard & mouse
- ✧ HP-HIL for input device loop
- ✧ Four phone jacks (microphone, headphones, line-in and ?)

4.28.4 ROM update

There is a firmware update available for the J200 & J210, which contains the latest version (2.0).

- ✧ PF_CJ2X0020.txt¹³² has details about the contents and installation of the patch.
- ✧ PF_CJ2X0020¹³³ contains the patch.

There is also a firmware update available for the J280 & J282, which contains the latest version (2.5).

- ✧ PF_CJ28X025.txt¹³⁴ has details about the contents and installation of the patch.
- ✧ PF_CJ28X025¹³⁵ contains the patch.

There is also a firmware update available for the J2240, which contains the latest version (2.1).

- ✧ PF_CJ224021.txt¹³⁶ has details about the contents and installation of the patch.
- ✧ PF_CJ224021¹³⁷ contains the patch.

¹³²ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ2X0020.txt

¹³³ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ2X0020

¹³⁴ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ28X025.txt

¹³⁵ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ28X025

¹³⁶ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ224021.txt

¹³⁷ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ224021

4.28.5 References

Manuals

- ◇ Visualize J200, J210 technical reference manual¹³⁸ (PDF, 2.6MB)
- ◇ Visualize J280 Owner's Guide¹³⁹ (PDF, 6.3MB)
- ◇ Visualize J280 workstation upgrade instructions¹⁴⁰ (PDF, 1.9MB)
- ◇ Visualize J280, J282, J2240 Service Handbook¹⁴¹ (PDF, 6.8MB)
- ◇ Visualize J282, J2240 Owner's Guide¹⁴² (PDF, 3.1MB)
- ◇ Visualize J282 workstation upgrade instructions¹⁴³ (PDF, 2.3MB)
- ◇ Visualize J2240 workstation upgrade instructions¹⁴⁴ (PDF, 1MB)

Articles

- ◇ Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost¹⁴⁵ (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- ◇ A New Memory System Design for Commercial and Technical Computing Products¹⁴⁶ (.pdf) Thomas R. Hotchkiss, Norman D. Marschke, and Richard M. McClosky (Februar 1996: Hewlett-Packard Journal)

Other

- ◇ Replacing the EEPROM on an HP Visualize J282¹⁴⁷ (HTML). In case your J-Class needs a new EEPROM chip (which is the case if it displays

FLT 3004
PDH

on its LCD display)

4.28.6 Operating systems

- ◇ HP-UX:
 - 10.20
 - 11.00 (minimum EP9808 for 64-bit environment on systems with 64-bit processors) and

¹³⁸<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37962/lpv37962.pdf>

¹³⁹<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37675/lpv37675.pdf>

¹⁴⁰<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38001/lpv38001.pdf>

¹⁴¹<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37964/lpv37964.pdf>

¹⁴²<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37966/lpv37966.pdf>

¹⁴³<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37965/lpv37965.pdf>

¹⁴⁴<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37963/lpv37963.pdf>

¹⁴⁵<http://www.hpl.hp.com/hpjournal/96feb/feb96a1.pdf>

¹⁴⁶<http://www.hpl.hp.com/hpjournal/96feb/feb96a5.pdf>

¹⁴⁷<http://www.lava.net/~kirill/j282/eprom.html>

- 11.00 and 11i
- ◇ Linux: works fine
- ◇ OpenBSD works (only 32-bit on the 64-bit PA-8x00 systems; the 53C720 Fast-Wide HVD SCSI controller is supported since release 4.2)

4.28.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
J200	4.98	4.50	44.8	61.3
J200 2-CPU			64.5	105
J210	6.00	5.40	54.0	73.4
J210 2-CPU			77.5	126
J210XC	6.40	5.70	57.6	81.5
J210XC2-CPU			82.8	142
J280	11.80	19.30		
J282	?	?		
J2240	17.40	26.30	157	237
J2240 2-CPU			307	349

4.28.8 Physical dimensions/Power

- ◇ 470×330×541mm height/width/depth
- ◇ 36kg net weight, 49.9kg fully loaded
- ◇ 1150W max. power input
- ◇ 6A max. RMS at 240V
- ◇ 12A max. RMS at 120V

4.29 HP Visualize J5000, J5600, J7000 & J7600

4.29.1 Overview

These workstations were aimed at the graphics workstations market, equipped with up to two 64-bit PA-8500 featuring large on-chip L1 caches. They are basically the bigger brothers of the C3000/C3600 et al, featuring better expandability. The architecture was a major change from those of its predecessors, e.g., the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports. The case also was a major redesign.

Model numbers: all have the HP 9000/785 model number.

4.29.2 Internals

CPU

- ◇ J5000: 1-2 PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ J5600: 1-2 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ J7000: 1-4 PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ J7600: 1-4 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache each

Chipset

- ◇ Astro memory/Runway controller
- ◇ Four Elroy PCI bridges
- ◇ National 87560 (*SuperI/O*), handling USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- ◇ Runway CPU/memory bus
- ◇ PCI-64/33 high-performance device I/O bus
- ◇ PCI-64/66 high-performance graphics I/O bus
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ SCSI-3 Ultra2-Wide LVD bus main storage I/O
- ◇ IDE bus; CD/floppy I/O

Memory

- ◇ 278-pin 120MHz ECC SDRAM DIMMs
- ◇ Takes 256/512/1024MB modules
- ◇ J5000: 8 slots
- ◇ J7000: 16 slots
- ◇ 256MB (1×256) minimum, J5000: 8GB (8×1024) maximum; J7000: 16GB (16×1024) maximum.

Expansion

- ◇ Five PCI 64-bit/33MHz, 5V slots
- ◇ Two PCI 64-bit/66MHz, 3.3V slots
- ◇ I/O slots layout (from top to bottom):
 1. EMPTY
 2. PCI-64/33, 5V
 3. PCI-64/33, 5V
 4. PCI-64/66, 3.3V
 5. PCI-64/33, 5V
 6. PCI-64/33, 5V
 7. PCI-64/66, 3.3V
 8. PCI-64/33, 5V

Drives

- ◇ One tray for four 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector
- ◇ One tray for a 3.5" Floppy drive
- ◇ One tray for a half-height 5.25" SCSI drive, external accessible

4.29.3 External connectors

- ◇ 50-pin HD SCSI-2 Ultra-Narrow single-ended
- ◇ 68-pin HD SCSI-3 Ultra2-Wide LVD
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ Two USB ports for keyboard & mouse

- ✧ Four phone jacks (microphone, headphones, line-in and line-out)

4.29.4 ROM update

There is an firmware update available which contains the latest version (5.0).

- ✧ PF_CBCJ0050.txt¹⁴⁸ has details about the contents and installation of the patch.
- ✧ PF_CBCJ0050¹⁴⁹ contains the patch.

4.29.5 References

Manuals

- ✧ J5x00/J7x00 Owner's Guide¹⁵⁰ (PDF, 4.5MB)
- ✧ J5x00/J7x00 Service Handbook¹⁵¹ (PDF, 4.4MB)
- ✧ VISUALIZE Workstation Memory Subsystem¹⁵² (PDF, 120KB)

4.29.6 Operating systems

- ✧ HP-UX:
 - J5000: 10.20 minimum *ACE 9906*
 - 10.20 minimum *ACE 9912* [unclear if J7600 also supports 10.20 — *Ed.*]
 - 11.00 minimum *EP 9808* [not sure — *Ed.*] or *ACE9911*, and *11i v1* (both only 64-bit releases)
- ✧ Linux: works.
- ✧ OpenBSD (32-bit): works.

4.29.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp	SPEC2000, int	SPEC2000, fp
J5000	32.50	54.00	302	486		
J50002-CPU			579	744		
J5600	42.60	62.70	384	564	408	392
J56002-CPU			758	847		
J7000	32.50	54.00	302	486		
J70002-CPU			579	744		

¹⁴⁸http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt

¹⁴⁹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050

¹⁵⁰<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37967/lpv37967.pdf>

¹⁵¹<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37674/lpv37674.pdf>

¹⁵²<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf>

4.30 HP Visualize J6000 & J6700

4.30.1 Overview

These small workstations were aimed at the graphics workstations market, equipped with the new 64-bit PA-8600 and PA-8700, both featuring large on-chip L1 caches. The architecture was a major change from those of its predecessors. New I/O devices were integrated, the LASI I/O chip was dumped together with the old GSC bus. All these devices now sit on several PCI buses, human I/O devices are connected to USB ports. The case can be used on the desktop or fitted in a 19" rack (2U).

Model numbers: all have the HP 9000/785 model number.

4.30.2 Internals

CPU

- ◇ J6000: 1-2 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache
- ◇ J6700: 1-2 PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache
- ◇ J6750: 1-2 PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache

Chipset

The system is built around the HP Astro chipset:

- ◇ HP Astro chipset
 - **Astro memory and I/O controller** connects to the two processors via the Runway processor bus (2.0GB/s), the memory bus (2.0GB/s) and eight I/O channels (“ropes” — aggregate 2.0GB/s) and contains both memory, I/O and cache controllers
 - Four **Elroy PCI bridges** connect the PCI slots and I/O devices on the onboard PCI bus to the Astro with an aggregate bandwidth of 2.0GB/s on seven I/O channels (one of the eight channels of the Astro controller is unused)
 1. PCI 64/66 I/O slot on two channels — 0.5GB/s
 2. PCI 64/66 I/O slot on two channels — 0.5GB/s
 3. PCI 64/66 I/O slot on two channels — 0.5GB/s
 4. Onboard I/O devices (Fast Ethernet, SCSI, audio, IDE/USB etc.) on one channel — 250MB/s
- ◇ National 87560 (“Super I/O”), integrates USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- ◇ Runway CPU bus with 2.0GB/s
- ◇ Memory bus, about 2.0GB/s
- ◇ I/O bandwidth of around 1.75GB/s
- ◇ Three PCI-64/66 buses for expansion slots
- ◇ PCI-64/33 bus for onboard I/O devices
- ◇ SCSI-3 Ultra2-Wide LVD buses main storage I/O
- ◇ IDE bus for CD/DVD removable media

Memory

- ◇ 278-pin 120MHz ECC SDRAM DIMMs
- ◇ 16 slots
- ◇ Takes 512MB/1GB DIMMs
- ◇ 1GB (2×512) minimum, 16GB maximum (16×1G)

Expansion

- ◇ Three PCI 64-bit/66MHz, 3.3V slots

Drives

- ◇ One tray for two 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector
- ◇ One tray for a slim-line ATAPI CD-ROM

4.30.3 External connectors

- ◇ 68-pin HD SCSI-3 Ultra2-Wide LVD connector (SE)
- ◇ Two DB9 male RS232C serial
- ◇ DB25 female parallel
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ Two USB ports for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

4.30.4 ROM update

There is a firmware update available for the **PA-8600**-based J6000, which contains the latest version (5.0).

◇ **PF_CBCJ0050.txt**¹⁵³ has details about the contents and installation of the patch.

◇ **PF_CBCJ0050**¹⁵⁴ contains the patch.

A different firmware update is provided for the **PA-8700**-based J6700 systems (version 2.0):

◇ **PF_CCJ70020.txt**¹⁵⁵ has details about the contents and installation of the patch.

◇ **PF_CCJ70020**¹⁵⁶ contains the patch.

4.30.5 References

Manuals

◇ **J6000 Service Handbook**¹⁵⁷ (PDF, 4.5MB)

◇ **J6000 Technical Reference**¹⁵⁸ (PDF, 3.3MB)

◇ **J6700 Service Handbook**¹⁵⁹ (PDF, 9.8MB)

◇ **J6700 Technical Reference**¹⁶⁰ (PDF, 5.6MB)

4.30.6 Operating systems

◇ **HP-UX:**

– J6000: 10.20 *ACE 9912*

– 11.00 minimum *EP 9808* [not sure—*Ed.*] or *ACE9911*, and 11i v1 (both only 64-bit releases)

◇ **Linux:** works.

◇ **OpenBSD (32-bit):** works.

4.30.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95 <i>rate</i> , int	SPEC95 <i>rate</i> , fp	SPEC2000, int	SPEC2000, fp	SPEC2000 <i>rate</i> , int	SPEC2000 <i>rate</i> , fp
J6000	42.60	62.70	384 2-CPU: 758	564 2-CPU: 847	441	433	2-CPU: 9.7	2-CPU: 8.0

¹⁵³http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt

¹⁵⁴http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050

¹⁵⁵http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020.txt

¹⁵⁶http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020

¹⁵⁷<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37677/lpv37677.pdf>

¹⁵⁸<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37634/lpv37634.pdf>

¹⁵⁹<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37640/lpv37640.pdf>

¹⁶⁰<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37641/lpv37641.pdf>

J6700	57.60	85.90			603	581	2-CPU: 13.4	2-CPU: 10.5
J6750					676	651	2-CPU: 14.9	2-CPU: 11.5

4.3.1 HP 9000/K-Class

4.3.1.1 Overview

The K-Class *Hawk* servers except the K100 are multiprocessor systems. The K370/K380 and K570/K580 are able to support up to six-way multiprocessing, whereas the K2x0 and K4x0 support up to four-way SMP. A typical K-Class server consists of a *System Processing Unit* (SPU), system console and an optional *Uninterruptible Power Supply* (UPS). These units then are packaged in a 19" rack.

- ✧ The first number after the “K” — 1, 2, 3, 4 or 5 — indicates the general type:
 - K100 are single-CPU with limited expandability
 - K2x0 take up to four CPUs, better expandability (more RAM) than K100
 - K3x0 take up to six CPUs, more I/O slots than K2x0
 - K4x0 take up to four CPUs, more I/O slots and partially more RAM than K2x0
 - K5x0 take up to six CPUs, different I/O configuration than K3x0
- ✧ The latter numbers [00, 10, ..., 80] indicate the “internal” features, like CPU and chipset.

Model numbers and introductions dates:

System	Model number	Introduced
K100, K200, K400	HP 9000/809, HP 9000/819, HP 9000/829	March 1995
K210, K410	HP 9000/839, HP 9000/849	September 1995
K220, K420	HP 9000/859, HP 9000/869	March 1996
K250, K450	HP 9000/802, HP 9000/804	August 1996
K260, K460	HP 9000/879, HP 9000/889	August 1996
K370, K570	HP 9000/898, HP 9000/899	May 1997
K380, K580	HP 9000/800	February 1998

4.3.1.2 Internals

CPU

- ✧ K100: PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache
- ✧ K200/K400: 1-4 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache each
- ✧ K210/K410: 1-4 PA-7200 120MHz with 256/256KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache each
- ✧ K220/K420: 1-4 PA-7200 120MHz with 1024/1024KB off-chip I/D L1 and 2KB on-chip “assist” L1 cache each
- ✧ K250/K450: 1-4 PA-8000 160MHz with 1024/1024KB off-chip I/D L1 cache each
- ✧ K260/K460: 1-4 PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache each
- ✧ K370/L570: 1-6 PA-8200 200MHz with 2048/2048KB off-chip I/D L1 cache each
- ✧ K380/K580: 1-6 PA-8200 240MHz with 2048/2048KB off-chip I/D L1 cache each

The 2KB on-chip “assist” cache on systems with a PA-7200 is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ PA-7200-models: U2 I/O adapter Runway to GSC bridge
- ◇ PA-8000/PA-8200-models: UTurn I/O adapter Runway to GSC bridge
- ◇ PA-7200/PA-8000/PA-8200 models: MMC/SMC memory controllers
- ◇ Gecko BOA BC GSC+ Port
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- ◇ Eole CAP/MUX

Buses

- ◇ Runway CPU/memory bus (100MHz with 800MB peak data rate on Kx00, 120MHz 960MB/s on all others)
- ◇ GSC+ bus for the general system level I/O
- ◇ HSC bus for expansion I/O
- ◇ HP-PB bus for expansion I/O
- ◇ SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- ◇ SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Memory

- ◇ 72-pin ECC SIMMs on special RAM boards

The required access-time of the RAM modules depends on the used CPU in the system, systems with a PA-8x00 need 50ns modules, those with PA-7200 and can take up to 60ns. It is possible that slower modules will also work.

Expansion

K100/K2x0:

- ◇ One slot for a GSC/HSC (HSC formfactor) card on the core I/O board

- ◇ Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

K₃xo:

- ◇ One slot for a GSC/HSC (HSC formfactor) card on the core I/O board
- ◇ Through the use of an 2-slot HSC I/O expansion module, which can be installed at the rear into the slot right of the core I/O, these models can facilitate two more GSC/HSC (HSC formfactor) cards.
- ◇ Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

K₄xo:

- ◇ One slot for a GSC/HSC (HSC formfactor) card on the core I/O board
- ◇ Through the use of an 2 or 4-slot HSC I/O expansion module, which can be installed at the rear into the slot right of the core I/O, these models can facilitate two or four more GSC/HSC (HSC formfactor) cards.
- ◇ Eight slots for HP-PB cards, from which four slots can either be used for single or double-height HP-PB cards.

K₅xo:

- ◇ One slot for a GSC/HSC (HSC formfactor) card on the core I/O board
- ◇ Through the use of an 2 or 4-slot HSC I/O expansion module, which can be installed at the rear into the slot right of the core I/O, these models can facilitate two or four more GSC/HSC (HSC formfactor) cards.
- ◇ Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

Drives

- ◇ One tray for four Fast-Wide 68-pin SCSI-2 high-voltage differential hard drives
- ◇ One vertical tray for two 5.25" half-height drives, external accessible

4.31.3 External connectors

- ◇ 68-pin HD SCSI-2 Fast-Wide high-voltage differential
- ◇ TP/RJ45 10BaseT 10Mbit Ethernet
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ Two DB9 male RS232C serial, one for console, one for UPS
- ◇ DB25 male RS232C serial, for remote console via modem
- ◇ DB25 female parallel
- ◇ Two PS/2 connectors for keyboard und mouse
- ◇ MDP-connector for a serial MUX

- ◇ Kx50/Kx60/Kx70/Kx80: four audio jacks

4.3.1.4 ROM update

There is a firmware update available for the K200, Kx10, Kx20 and K400 which contains the latest version (2.9).

- ◇ PF_CKHK0029.txt¹⁶¹ has details about the contents and installation of the patch.
- ◇ PF_CKHK0029¹⁶² contains the patch.

There is a firmware update available for the Kx50/Kx60 which contains the latest version (39.43).

- ◇ PF_CMHK3943.txt¹⁶³ has details about the contents and installation of the patch.
- ◇ PF_CMHK3943¹⁶⁴ contains the patch.

There is a firmware update available for the Kx60 which contains the latest version (41.33).

- ◇ PF_CMHK4133.txt¹⁶⁵ has details about the contents and installation of the patch.
- ◇ PF_CMHK4133¹⁶⁶ contains the patch.

4.3.1.5 References

Manuals

- ◇ Service Manual HP 9000 K-Class Enterprise Servers and HP 3000 Model 9x9KS¹⁶⁷ (PDF, 2.1MB)
- ◇ K-Class Installation Guide (HP 9000/Kxx0)¹⁶⁸ (PDF)
- ◇ K-Class Installation Guide (HP 3000/9x9KS)¹⁶⁹ (PDF)
- ◇ K-Class Owner's Guide¹⁷⁰ (PDF)
- ◇ K-Class System Upgrade Manual¹⁷¹ (PDF)

Articles

- ◇ Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost¹⁷² (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- ◇ J/K-Class Memory System description¹⁷³ (PDF, HP Journal 2/96)

¹⁶¹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKHK0029.txt

¹⁶²http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKHK0029

¹⁶³http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK3943.txt

¹⁶⁴http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK3943

¹⁶⁵http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK4133.txt

¹⁶⁶http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK4133

¹⁶⁷<http://ftp.parisc-linux.org/docs/platforms/A2375-90004.pdf>

¹⁶⁸<http://docs.hp.com/hpux/pdf/A2375-90006.pdf>

¹⁶⁹<http://docs.hp.com/hpux/pdf/A2375-90005.pdf>

¹⁷⁰<http://docs.hp.com/hpux/pdf/A2375-90003.pdf>

¹⁷¹<http://docs.hp.com/hpux/pdf/A2375-90011.pdf>

¹⁷²<http://www.hpl.hp.com/hpjjournal/96feb/feb96a1.pdf>

¹⁷³<http://www.hpl.hp.com/hpjjournal/96feb/feb96a5.pdf>

4.31.6 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works. Systems with a 64-bit PA-8x00 CPU also can use 64-bit version of HP-UX 11.x.
 - 10.20 for 800s servers: runs very nicely.
 - 11.00 and 11i v1: run nicely
- ◇ Linux: works on most models.
- ◇ OpenBSD: on-going work to support at least the K220.

4.31.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPeCrate95, int	SPeCrate95, fp
Kx00	4.92	6.80	44.3	61.2
Kx002-CPU			87.9	117
Kx004-CPU			174	198
Kx10	5.92	8.15	53.3	73.4
Kx102-CPU			106	140
Kx104-CPU			210	238
Kx20	6.41	9.11	57.7	82.0
Kx202-CPU			114	157
Kx204-CPU			228	275
Kx50	10.7	18.8	96.	169
Kx502-CPU			189	279
Kx504-CPU			375	383
Kx60	11.8	20.2	107	182
Kx602-CPU			212	297
Kx604-CPU			418	398
Kx70	14.6	23.0	132	207
Kx702-CPU			261	322
Kx704-CPU			519	434
Kx706-CPU			767	489
Kx80	17.4	28.5	157	257
Kx802-CPU			312	398
Kx804-CPU			610	532
Kx806-CPU			902	604

4.31.8 Physical dimensions/Power

Stand-alone:

- ◇ 635×432×698 mm height/width/depth
- ◇ 59kg weight

Packaged:

- ◇ 870×889×775 mm height/width/depth
- ◇ 76.66kg

Kx00/Kx10/Kx20:

- ◇ 1250W max. power input, 450W typical
- ◇ 6A max. RMS at 240V

◇ 10.5A max. RMS at 120V

Kx50/Kx60/Kx70:

◇ 2400W max. power input

◇ 10A max. RMS at 240V

◇ 16A max. RMS at 120V

◇ Require 20A power services.

4.32 HP i2000

4.32.1 Overview

The HP i2000 was HP's first Itanium workstation with a first generation Itanium processor (*Merced*) and more a proof-of-concept to deliver first Itanium hardware, based on an early Intel reference design (which was also rebranded and sold by other vendors). The system had certain limitations (some due to chipset/OS bugs), supported only first generation Itanium CPUs and was rather slow.

Time of introduction: 2001, with price at the time of \$7,000 to \$15,000.

4.32.2 Internals

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1	Itanium 1 <i>Merced</i>	733MHz	16/16KB	96KB	2.0MB or 4.0MB
1-2	Itanium 1 <i>Merced</i>	800MHz	16/16KB	96KB	2.0MB or 4.0MB

L1 and L2 caches are on-die, L3 is off-chip

Chipset

- ◇ Intel 82460GX chipset
- ◇ Two WXBs (Wide eXpansion Bridges) for each one PCI 64/66 bus
- ◇ PXB (PCI eXpansion Bridge) for one PCI 64/33 bus
- ◇ I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- ◇ Qlogic 12160 dual-channel Ultra3 SCSI controller (separate PCI card, standard configuration)
- ◇ Intel 82559 Fast Ethernet controller
- ◇ nVIDIA Quadro2 Pro video card (separate AGP card, standard configuration)
- ◇ ATA-33 IDE controller (on IFB)
- ◇ USB controller (on IFB)
- ◇ LPC47B27 Super I/O (serial and PS/2 ports controller)

Buses

- ◇ Memory bus, 266MHz, 4.2GB/s peak
- ◇ Two PCI 64/66 I/O buses (for expansion slots)
- ◇ PCI 64/33 I/O bus (for expansion slots)
- ◇ PCI 32/33 I/O bus (for onboard devices)

Memory

- ◇ PC100 registered SDRAM DIMMs
- ◇ Up to two memory expansion cards (MECs)
- ◇ Eight slots on each MEC
- ◇ Up to 1GB modules
- ◇ 16GB maximum (16×1GB—8GB on each MEC) [some say 16GB is not supported—not sure what that means]

Expansion

- ◇ Five PCI 64-bit/66MHz slots, 3.3V
- ◇ Two PCI 64-bit/33MHz slots, 5V
- ◇ One AGP Pro 110 slot (supports AGP-1X, 3X, 4X, or AGPpro-110)

Drives

- ◇ Three (1.6") or five (1") internal 3.5" bays for hard drives
- ◇ Three half-height 5.25" bays for externally accessible drives
- ◇ One 3.5" bay for externally accessible drive (standard shipped with a LS-120 drive)

4.32.3 External connectors

- ◇ 10/100 Ethernet TP/RJ45
- ◇ Four USB ports (two on front, two on rear)
- ◇ DB9 male RS232C serial
- ◇ Two PS/2 for keyboard and mouse
- ◇ Three phone jacks (microphone, line-in and line-out)

4.32.4 References

Manuals

- ◇ **HP Workstation i2000 Owner's Guide**¹⁷⁴ (PDF) Hewlett-Packard Company (May 2001, first edition)

¹⁷⁴<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpv37642/lpv37642.pdf>

4.32.5 Operating systems

- ◇ HP-UX 11i v1.5 and v1.6 (later versions do not work) — due to a chipset bug HP-UX does not support a (local) X server on the i2000
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ Windows XP Professional 64-bit Edition
- ◇ Windows 2000 Server IA64 Edition (Beta Release)
- ◇ Windows Server 2003 Itanium-based Editions

4.32.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
i2000733MHz 2MB		623		7.2
i2000733MHz 4MB		577		
i2000800MHz 2MB		6552-CPU: 658		7.6 2-CPU: 13.2
i2000800MHz 4MB	365	610		

4.32.7 Physical dimensions/Power

- ◇ 457×254×645 mm height (with feet)/width/depth
- ◇ 38kg weight
- ◇ 800W max. power input

4.33 HP L1000 & L2000 (rp5400/rp5450) Servers

4.33.1 Overview

These 7U rack-mountable SMP servers supported either up to two (L1000/rp5400) or up to four (L2000/rp5450) 64-bit PA-RISC processors. In contrast to their L1500/L3000 successors the L1000/L2000 were based on a rather conservative system architecture, using the Astro/Elroy main chipset combination used in many other *four-digits* workstations and servers.

The L1000 and L2000 could be upgraded with a board-swap (mainboard, processors, etc.) to the Itanium 2-based rx5670 servers.

Introduced: October 1999.

Model numbers:

- ◇ L1000-36, L1000-44, L1000-5X: rp5400
- ◇ L2000-36, L2000-44, L2000-5X: rp5450

4.33.2 Internals

CPU

Both the L1000 and L2000 came with two different system boards, which supported different types of processors (A versus B suffix on the model number).

- ◇ L1000 (rp5400): up to two CPUs, with the processor type depending on the exact model number:
 - A5576A: 360MHz and 440MHz processors
 - A5576B: 360MHz, 440MHz and 550MHz processors
- ◇ L2000 (rp5450): up to four CPUs, with the processor type depending on the exact model number:
 - A5191A: 360MHz and 440MHz processors
 - A5191B: 360MHz, 440MHz and 550MHz processors

The L1000/rp5400 systems support up to 2-way and the L2000/rp5450 up to 4-way SMP. The following table lists the various suffixes denoting the different theoretically possible CPU-configurations. Upgrading from one configuration to another could require the replacement of other parts besides the processor, *e.g.*, the mainboard or power supply.

- ◇ -36: PA-8500 360MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ -44: PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each

It is possible not all system boards shipped with these L1000/L2000s support all possible processors.

Chipset

- ◇ Astro memory/Runway controller, connects the memory, CPU bus and I/O
- ◇ Eight Elroy PCI bridges

- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Two Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- ◇ Runway CPU bus, 82.5MHz with 1.36GB/s bandwidth for up to four CPUs
- ◇ Memory bus, 1.36GB/s
- ◇ Eight I/O data channels, each 133MHz 256MB/s — 2.1GB/s aggregate
- ◇ Two PCI-64/33 I/O buses
- ◇ Six PCI-64/66 I/O buses
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ◇ ECC SDRAM DIMMs
- ◇ Take 256MB/512MB modules
- ◇ 16 slots (*8 of these slots are disabled on L1000s, namely slots 4a/b, 5a/b, 6a/b and 7a/b*)
- ◇ 256MB (1×256) minimum, L1000: 8GB (8×1GB) maximum; L2000: 16GB (16×1GB) maximum.

Expansion

- ◇ Six PCI 64-bit/33MHz slots on two independent buses:
 - pcio: Slots 1 and 2 are reserved for the Core I/O cards
 - pci1: Slots 3, 4, 5 and 6
 - All of the above slots are not hot-plug capable
- ◇ Six PCI 64-bit/66MHz slots, each on an independent bus. These are hot-plug capable.
- ◇ *On L1000s only the slots 1, 2, 3, 8, 9, 10, 11 and 12 are usable!*
- ◇ Slot layout (from bottom to top):
 1. PCI-64/33, pcio, reserved for core I/O
 2. PCI-64/33, pcio, reserved for core I/O
 3. PCI-64/33, pci1
 4. PCI-64/33, pci1
 5. PCI-64/33, pci1

6. PCI-64/33, pci1
7. PCI-64/66, pci2, hot-pluggable
8. PCI-64/66, pci3, hot-pluggable
9. PCI-64/66, pci4, hot-pluggable
10. PCI-64/66, pci5, hot-pluggable
11. PCI-64/66, pci6, hot-pluggable
12. PCI-64/66, pci7, hot-pluggable

Drives

- ◇ Four trays for each one 3.5" Ultra2-Wide LVD SCSI hard drive with 80-pin SCA connector
- ◇ One tray for a half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external accessible

4.33.3 External connectors

- ◇ 50-pin HD SCSI-2 Ultra-Narrow single-ended
- ◇ 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- ◇ DB9 male RS232C serial
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ TP/RJ45 10Mbit Ethernet *Web Console*

4.33.4 ROM update

There is an firmware update available which contains the latest version (44.28).

- ◇ PF_CRHW4428.txt¹⁷⁵ has details about the contents and installation of the patch.
- ◇ PF_CRHW4428.tar.gz¹⁷⁶ contains the patch.

There is also an firmware update available for the (revision A) GSP service processors which contains the latest version A.01.12.

- ◇ PF_CPREGSPA0112.txt¹⁷⁷ has details about the contents and installation of the patch.
- ◇ PF_CPREGSPA0112.tar.gz¹⁷⁸ contains the patch.

¹⁷⁵http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CRHW4428.txt

¹⁷⁶http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CRHW4428.tar.gz

¹⁷⁷http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.txt

¹⁷⁸http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.tar.gz

4.33.5 References

Manuals

- ◇ **rp5400 User Guide**¹⁷⁹ (HTML)
- ◇ **rp5400 User Guide**¹⁸⁰ (PDF)

4.33.6 Operating systems

- ◇ HP-UX: Only 64-bit 11.00 and 11i (v1 and v2) releases run. You need at least 11.0 ACE 9911 or 11i.
- ◇ Linux: works.

4.33.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC2000, int	SPEC2000, fp
L2000-44	33.70	47.20	?	?

4.33.8 Physical dimensions/Power

- ◇ 368×482×774mm height/width/depth
- ◇ rack-mounted: 7U height, 482×774mm width/depth
- ◇ 68kg net weight
- ◇ Up to three hot-swappable power supplies
- ◇ Each has 930W max. power input

¹⁷⁹<http://www.docs.hp.com/hpux/onlinedocs/A5191-96018/A5191-96018.html>

¹⁸⁰<http://www.docs.hp.com/hpux/pdf/A5191-96018.pdf>

4.34 HP L1500 & L3000 (rp5430/rp5470)

4.34.1 Overview

The second incarnation of the L-Class servers are, similar to their direct predecessors L1000 and L2000, 7U rack-mountable servers with either 1-2 or 1-4 processors, 8GB or 16GB RAM and a large set of I/O options and expandability. The internal system architecture of the L1500 and L3000 is different however—the central parts of the processor/memory and I/O system were modified (trimmed-down) versions of the “Stretch” chipset used in the rp7400 N4000 servers.

The L1500 features the same chassis and mainboards as the L3000, however a large set of the interfaces (I/O, memory, processors sockets) is deactivated in hardware, limiting the L1500 to about half of the L3000’s expansion options.

These systems only run 64-bit versions of HP-UX—11.00 and 11i (v1 and v2). Linux *could* be usable however it is unclear how solid the support is, as these machines and their architecture were rather uncommon.

The L1500 and L3000 could be upgraded with a board-swap (mainboard, processors, etc.) to the Itanium 2-based rx5670 servers.

Introduced: 2001-2002

- ◇ L1500-36, L1500-44, L1500-5X, L1500-6X, L1500-7X, L1500-8X: rp5430
- ◇ L3000-5X, L3000-6X, L3000-7X, L3000-8X: rp5470

4.34.2 Internals

CPU

The rp5430 (L1500) support up to 2-way and the rp5470 (L3000) up to 4-way multi-processing (SMP). There are several classes of possible processors, both shipped with the systems or later upgraded. Support for individual processors depends on the specific system with corresponding firmware revisions, operating system support and, lastly, the system’s support/auxiliary hardware (power supplies, voltage changers, etc.).

Both the L1500 and L3000 came with different system boards, which supported different types of processors:

- ◇ L1500 (rp5430): up to two CPUs, system boards support all processors from 550MHz to 750MHz
- ◇ L3000 (rp5470): up to four CPUs, with the processor type depending on the exact model number [unsure which models support the 875MHz PA-8700+]:
 - A6144A: 550MHz processors
 - A6144B: 550MHz, 650MHz and 750MHz processors
 - A6840A: 550MHz, 650MHz and 750MHz processors
 - A8328A: 550MHz, 650MHz and 750MHz processors

Processor types are indicated with the following suffixes:

- ◇ -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each

- ◇ -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -8X: PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache each

Mixing different processors/speeds is not supported.

Chipset

The chipset is similar to the one used in the rp7400 N4000 servers, based around the “Stretch” chipset with a Prelude SMC memory controller which attaches to the memory and two system buses, which in turn connect up to four CPUs and the I/O controller(s).

- ◇ Stretch CEC (core electronics complex) — describes the complete chipset package of Prelude memory controller, DEW Runway converters and IKE I/O controller
- ◇ Prelude SMC memory controller
- ◇ DEW BC Runway converters (probably two — note quite clear from the whitepapers/descriptions, at least two would make sense)
- ◇ IKE I/O controller, connects the PCI bridges to the system main bus (to the left system main bus in fact — the right system bus is used exclusively by two CPUs while the left one is shared between CPUs and I/O)
- ◇ rp5430: Seven Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- ◇ rp5470: Ten Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Dual-channel Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- ◇ Two system buses, 133MHz, each 2.1GB/s peak — about 4.3GB/s aggregate (the system bus is in fact formally an Itanium/Merced system bus), with one system bus connecting the I/O and two CPUs and the other system bus connecting (only) two CPUs
- ◇ Two or four Runway+/Runway DDR CPU buses, each 2.1GB/s peak — aggregate 4.3 or 8.6GB/s peak (these Runway buses are attached to the two system buses — this means the CPUs have a theoretical bandwidth which cannot be sustained by the system’s main bus)
- ◇ Memory bus, 4.3GB/s
- ◇ rp5430:
 - Eight I/O data channels, each 133MHz 256MB/s — 2.1GB/s aggregate
 - Five PCI-64/66 I/O buses for expansion slots
 - One PCI-64/33 I/O bus for core I/O
- ◇ rp5470:

- Twelve I/O data channels, each 133MHz 256MB/s — 3.2GB/s aggregate
- Eight PCI-64/66 I/O buses for expansion slots
- Two PCI-64/33 I/O buses for expansions slots and core I/O
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ◇ ECC SDRAM DIMMs
- ◇ 256MB, 512MB and 1GB modules supported
- ◇ 16 slots
- ◇ rp5430: 8.0GB maximum (the system will not boot if more than 8.0GB of memory is installed)
- ◇ rp5470: 16.0GB maximum

Expansion

- ◇ Two “Twin-Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via two I/O data channels (aggregate 512MB/s), hot-plug capable
- ◇ rp5430:
 - Four “Turbo” PCI 64-bit/66MHz slots on three PCI buses, each connected via one I/O data channel (256MB/s), three of four slots are hot-plug capable
- ◇ rp5470:
 - Six “Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via one I/O data channel (256MB/s), hot-plug capable [two of these slots are not active on the rp5430]
 - Two PCI 64-bit/33MHz slots on a shared bus, on one I/O data channel (256MB/s) [these slots are not active on the rp5430]
- ◇ Two PCI 64-bit/33MHz slots, reserved for LAN/SCSI and GSP (management) cards, on a shared bus, on one I/O data channel (256MB/s)
- ◇ All PCI slots are 5V keyed
- ◇ Slot layout (counted from bottom up):
 1. PCI-64/33, pcio, reserved (LAN/SCSI)
 2. PCI-64/33, pcio, reserved (GSP)
 3. PCI-64/33, pci1, shared [not available on rp5430]
 4. PCI-64/33, pci1, shared [not available on rp5430]
 5. PCI-64/66, pci2, Turbo, hot-pluggable [not available on rp5430]
 6. PCI-64/66, pci3, Turbo, hot-pluggable [not available on rp5430]

7. PCI-64/66, pci4, Turbo, hot-pluggable
8. PCI-64/66, pci5, Turbo, hot-pluggable
9. PCI-64/66, pci6, Turbo, hot-pluggable
10. PCI-64/66, pci7, Turbo, hot-pluggable
11. PCI-64/66, pci8, Twin-Turbo, hot-pluggable
12. PCI-64/66, pci9, Twin-Turbo, hot-pluggable

Drives

- ◇ Four trays for 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector, hot-plug
- ◇ One tray for a half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external accessible

4.34.3 External connectors

- ◇ 50-pin HD SCSI-2 Ultra-Narrow single-ended
- ◇ 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- ◇ Three DB9 male RS232C serial (local console, remote console, general purpose)
- ◇ TP/RJ45 10/100Mbit Ethernet
- ◇ TP/RJ45 10/100Mbit Ethernet *Web Console*

4.34.4 ROM update

There is an firmware update available which contains the latest version (44.12).

- ◇ PF_CARIW4412.txt¹⁸¹ has details about the contents and installation of the patch.
- ◇ PF_CARIW4412.tar.gz¹⁸² contains the patch.

There is also an firmware update available for the revision A GSP service processors on the A6144A L3000 which contains the latest version A.01.12.

- ◇ PF_CPREGSPA0112.txt¹⁸³ has details about the contents and installation of the patch.
- ◇ PF_CPREGSPA0112.tar.gz¹⁸⁴ contains the patch.

There is also an firmware update available for the revision B GSP service processors on the L1500 and L3000 which contains the latest version B.02.20.

- ◇ PF_CCANGSPB0220.txt¹⁸⁵ has details about the contents and installation of the patch.
- ◇ PF_CCANGSPB0220.tar.gz¹⁸⁶ contains the patch.

¹⁸¹ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CARIW4412.txt

¹⁸²ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CARIW4412.tar.gz

¹⁸³ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.txt

¹⁸⁴ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.tar.gz

¹⁸⁵ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.txt

¹⁸⁶ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.tar.gz

4.34.5 References

Manuals

- ◇ **User Guide rp5400 Family of Servers**¹⁸⁷ (PDF) Hewlett-Packard Company (November 2002, first edition, product number 5981-2650EN)

Articles

- ◇ *hp server rp5400 series entry-level UNIX servers technical whitepaper*, Hewlett-Packard Company (August 2002) [did not find an appropriate URL for this PDF document — *Ed.*]

4.34.6 Operating systems

- ◇ HP-UX: 11.00 and 11i (v1 and v2)
- ◇ Linux: *should* work

4.34.7 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 <i>rate</i> , int	SPEC2000 <i>rate</i> , fp
L3000-5Xrp2470	388	376	4.52-CPU: 8.94-CPU: 17.4	4.42-CPU: 8.34-CPU: 14.5
L3000-7Xrp2470	581		6.7 2-CPU: 12.9	

4.34.8 Physical dimensions/Power

- ◇ 368×482×775mm height/width/depth
- ◇ Rack-mounted: 7U height, 482×775mm width/depth
- ◇ 68kg net weight
- ◇ Up to three hot-swappable power supplies (one is standard)
- ◇ Each has 930W max. power input

¹⁸⁷<http://docs.hp.com/en/A5191-96018/A5191-96018.pdf>

4.35 HP N4000 (rp7400)

4.35.1 Overview

The rp7400 were the original version of the N4000 line of servers—the newer rp7405 and rp7410 servers were also labeled as N4000 and feature a similar set of I/O options and expandability in basically the same chassis. However the original N4000, the rp7400 described here, is based around a different system architecture than their successors—the Stretch chipset, also used in the L1500 and L3000 (rp5430/rp5470) servers.

The original N4000s were shipped in two models, with differences in their system board—A3639A and A3639B. The N4000 which was later renamed to rp7400 was shipped with an even different mainboard and had the model number A3639C.

Introduced: 1999-2001

Model numbers: all the N4000-36, N4000-44, N4000-5X, N4000-6X and N4000-7X have the rp7400 model number.

4.35.2 Internals

CPU

The rp7400 N4000 supports one to eight processors.

The original N4000 (A3639A and A3639B) and later rp7400 (A3639C) are in fact different products, based on the same basic architecture but with slight differences, especially relating to the type and number of processors. Not all early N4000s support the later processors and a maximum number of CPUs.

Processor types are indicated with the following suffixes:

- ◇ -36: PA-8500 360MHz with 512/1024KB on-chip I/D L1 cache each [A3639A, A3639B, A3639C, A8327A]
- ◇ -44: PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each [A3639A, A3639B, A3639C, A8327A]
- ◇ -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each [A3639B, A3639C, A8327A]
- ◇ -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each [A3639C, A8327A]
- ◇ -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each [A3639C, A8327A]
- ◇ Itanium 2/IA64 processors were planned on the N4000 but apparently never offered.

Chipset

The rp7400 system is based on the Stretch central electronic complex chipset, used in the L1500 and L3000 (rp5430/rp5470) servers as well. Stretch has four main components, to which the processing and I/O parts of the N4000 attach:

1. **Prelude SMC memory controller** is the central part of the system, it connects the memory to two system buses, to which each one IKE I/O controller and two DEW Runway ports (for each two CPUs) attach (Prelude is also called “Very Low Latency Memory Controller”)

2. **Four DEW Runway ports/converters** convert the Prelude's system bus(es) (which in fact is an Itanium/Merced bus) into Runway buses for the up to eight CPUs—each two CPUs share one DEW port converter
3. **Two IKE I/O controllers** attach each to one system bus on one side and to eight (left IKE — system bus 0) or six (right IKE — system bus 1) PCI bridges
4. **14 Elroy PCI bridges** (LBAs) which convert the I/O channels from the IKE I/O controllers into PCI buses, to which the PCI slots and core I/O functions attach

The remainder of the system I/O is implemented with common parts also used in other HP 9000 servers:

- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Dual-channel Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

The system bus architecture is in some ways rather strange, as it provided much more theoretical bandwidth than could be used under practical circumstances. The designers probably counted on future CPU upgrades, such as Itanium processors.

- ◇ Two system buses, 133MHz, each 2.1GB/s peak—about 4.3GB/s aggregate (the system bus is in fact formally an Itanium/Merced system bus)
- ◇ Eight Runway+/Runway DDR CPU buses, each 2.1GB/s peak—aggregate 17.0GB/s peak (these Runway buses are attached to the two system buses—this means the CPUs have a theoretical bandwidth which cannot be sustained by the system's main bus)
- ◇ Four Memory buses, each 2.1GB/s peak—aggregate 8.5GB/s (interestingly, the memory bus bandwidth is much wider than the CPUs' maximum bus bandwidth, leaving room for anticipated CPU upgrades, which apparently never really materialized)
- ◇ 24 I/O data channels, each 133MHz 265MB/s—6.4GB/s aggregate
- ◇ 14 PCI-64/66 I/O buses for expansion slots
- ◇ Three SCSI-3 Ultra2-Wide LVD main storage I/O buses, one for each internal drive and one for external devices

Memory

- ◇ ECC SDRAM DIMMs
- ◇ 16 slots
- ◇ 256MB, 512MB, 1GB and 2GB modules supported
- ◇ 32GB maximum

Expansion

- ◇ 10 “Twin-Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via two I/O links/ropes (aggregate 530MB/s), hot-plug capable
- ◇ Two “Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via one I/O link/rope (265MB/s), hot-plug capable (one of these two Turbo slots is reserved for Core I/O LAN/SCSI)
- ◇ All slots keyed for 5.0V (support either 5.0V or universal PCI cards)

Drives

- ◇ Two internal Ultra SCSI LVD 3.5” drives with SCA connector, hot-pluggable

4.35.3 External connectors

- ◇ 68-pin VHDCI Ultra LVD external SCSI
- ◇ Three DB9 male RS232C serial (local console, remote console, general purpose) via a DB25 “M cable”
- ◇ 10/100Mbit Ethernet TP/RJ45
- ◇ 10/100Mbit Ethernet TP/RJ45 *LAN console*

4.35.4 ROM update

There is an firmware update available for the N4000/rp7400 (A3639A, A3639B, A3639C) which contains the latest version 43.43.

- ◇ PF_CPIW4343.txt¹⁸⁸ has details about the contents and installation of the patch.
- ◇ PF_CPIW4343.tar.gz¹⁸⁹ contains the patch.

There is also an firmware update available for the (revision A) GSP service processors on the original N4000 (A3639A and A3639B) which contains the latest version A.01.12.

- ◇ PF_CPREGSPA0112.txt¹⁹⁰ has details about the contents and installation of the patch.
- ◇ PF_CPREGSPA0112.tar.gz¹⁹¹ contains the patch.

There is also an firmware update available for the revision B GSP service processors on the A3639C rp7400 which contains the latest version B.02.20.

- ◇ PF_CCANGSPB0220.txt¹⁹² has details about the contents and installation of the patch.
- ◇ PF_CCANGSPB0220.tar.gz¹⁹³ contains the patch.

¹⁸⁸[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPIW4343.txt](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPIW4343.txt)

¹⁸⁹[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPIW4343.tar.gz](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPIW4343.tar.gz)

¹⁹⁰[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.txt](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.txt)

¹⁹¹[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.tar.gz](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CPREGSPA0112.tar.gz)

¹⁹²[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.txt](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.txt)

¹⁹³[ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.tar.gz](http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCANGSPB0220.tar.gz)

4.35.5 References

Manuals

- ◇ **rp7400 Hardware Manual**¹⁹⁴ (PDF) Hewlett-Packard Company (May 2002)

Articles

- ◇ *hp server rp7400 whitepaper*, Hewlett-Packard Company (February 2002, product number 5981-0154EN) [did not find an appropriate URL for this PDF document — *Ed.*]

4.35.6 Operating systems

- ◇ HP-UX: 11.00 and 11i (v1, v2 and v3)
- ◇ Linux: should work.

4.35.7 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 rate, int	SPEC2000 rate, fp
N4000-6X rp7400	493	489	5.7 2-CPU: 11.3 4-CPU: 22.1 8-CPU: 42.6	5.7 2-CPU: 10.4 4-CPU: 19.3 8-CPU: 30.5
N4000-7X rp7400	551	524	6.4 2-CPU: 12.5 4-CPU: 24.6 8-CPU: 46.7	6.1 2-CPU: 11.0 4-CPU: 20.5 8-CPU: 32.1

4.35.8 Physical dimensions

- ◇ Rack-mounted: 10U height
- ◇ Up to three power supplies — two are needed for the maximum configuration of CPUs, memory and drives, the third would be redundant

¹⁹⁴http://docs.hp.com/en/3687/rp7400_customer_hardwaremanual.pdf

4.36 HP N4000 (rp7405/rp7410)

4.36.1 Overview

The rp7405/rp7410 N4000 servers are up to 8-way multiprocessing servers and the smallest HP systems which can be partitioned into *logical* servers (two **nPartitions**). Based upon the same 10U rack-mountable chassis as their rp7400/N4000 brethren, the newer rp7405 and rp7410 are built around a completely overhauled system and I/O architecture. The “Core Electronic Complex” is a modified version of the Superdome’s cell-based system architecture, limited to two cells, which each contain up to four processors, sixteen memory slots and the central chipset—the cell controller (CC). These newer N4000s feature a very large amount of system and I/O bandwidth: 16GB/s CPU, 8GB/s memory, 8GB/s cell-to-cell and 8.5GB/s I/O bandwidth (all maximum aggregate values).

The rp7405 was apparently an entry-level version of the rp7410—based on the same hardware and with the same capabilities but shipped in smaller configurations. Upgrades to a “full” rp7410 were later possible, probably including a modified firmware for unlocking the full functionality.

Introduced: 1999-2000

4.36.2 Internals

CPU

The rp7405 and rp7410 support from two to eight processors.

They are based on different system boards with different model numbers—the same basic architecture but with differences relating to the type and number of processors.

- ◇ A6752A (rp7410) supports 650MHz, 750MHz and 875MHz processors
- ◇ A7111A (two-way rp7405) supports 650MHz and 750MHz processors
- ◇ A7112A (four-way rp7405) supports 650MHz and 750MHz processors
- ◇ A7113A (eight-way rp7405) supports 650MHz and 750MHz processors

Processor types are indicated with the following suffixes:

- ◇ -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -8X: PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache each
- ◇ -9X: PA-8800 (dual-core) 900MHz/1.0GHz with 1.5/1.5MB on-chip L1 and 32MB off-chip L2 cache each
- ◇ PA-8900 (dual-core) 800MHz-1.1GHz with 1.5/1.5MB on-chip L1 and 64MB off-chip L2 is probably also possible (suffix and affected models unknown)
- ◇ Itanium 2/IA64 processors are probably also possible on some models
- ◇ It is unclear which models support the -8X, -9X, PA-8900 and IA64 processors

There are two CPU/memory cell boards, with each four processor sockets.

Chipset

The Cell system architecture has three main components:

1. **Cell controller (CC):** the central chipset and crossbar. One sits at the centre of each cell board for a maximum of two in a complete system. The CCs provide links for:
 - ✧ Four Processors (8.0GB/s)
 - ✧ Two Memory “banks” (4.0GB/s peak)
 - ✧ I/O via SBA (cell to I/O communication is 2.0GB/s peak)
 - ✧ PDH (processor dependent hardware) and firmware/flash etc.
 - ✧ Second cell via XBC (cell-to-cell communication is 8.0GB/s peak)
2. **Master I/O controller (SBA):** the central I/O part of the main chipset. rp7405/rp7410 have two SBAs, located on the I/O backplane. Each is linked to one cell—with one cell board only one SBA and its I/O options can be used.
 - ✧ Each SBA provides sixteen 12-bit links (“ropes”)—the combined 32 (2×16) links/ropes from both SBAs connect to 18 slave I/O controllers (LBAs) which in turn connect the PCI I/O slots and Core I/O subsystems
 - ✧ 28 ropes link to 14 “Twin-Turbo” slots (via 14 LBAs)
 - ✧ Two ropes link to two “Turbo” (that is, normal) PCI slots (via two LBAs), from which one is reserved for the PCI Core I/O LAN/SCSI card
 - ✧ Two links/ropes (one from each SBA) are connected via two LBAs to the Core I/O MP/SCSI card(s)
3. **Core I/O card set:** provides the standard I/O functions for the system. One of these sets is the required minimum in any N4000, up to two Core I/O card sets are possible. Each Core I/O card set contains two distinct cards: MP/SCSI card, installed in a separate slot, and LAN/SCSI, installed in PCI slot (specially designated, I/O chassis 1, slot 8).
 - ✧ Two dual-channel Symbios Logic 53C1010 Ultra160 SCSI controllers (on MP/SCSI and LAN/SCSI)
 - ✧ Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller (MP/SCSI)
 - ✧ Gigabit Ethernet networking (LAN/SCSI)
 - ✧ Diva Serial [GSP] Multiport UART for console (MP/SCSI), serial and management controllers (MP/SCSI)
 - ✧ Fast-Ethernet (DEC 21142/43) Management LAN (MP/SCSI)
 - ✧ The optional second Core I/O card set can be used either for redundancy or partitioning purposes (I/O for the second partition)

Other parts of the chipset:

- ✧ Prelude SMC memory controllers (on each cell board)
- ✧ 18 Elroy PCI bridges (LBAs) convert the links/ropes from the SBA into PCI bus (only 9 of these 18 LBAs are used when only one cell board is installed)

Buses

- ◇ Runway+/Runway DDR CPU bus (CPU to cell controller), 125MHz DDR, 64-bit wide, 2.0GB/s *per CPU* — aggregate 8.0GB/s for each cell (four CPUs/cell) and 16.0GB/s for maximum system
- ◇ Memory bus (memory to cell controller) 4.0GB/s for each cell — aggregate 8.0GB/s for maximum system
- ◇ XBC cell-to-cell link (cell controller to cell controller) 8.0GB/s aggregate
- ◇ SBA cell-to-I/O link (cell controller to I/O backplane) 2.0GB/s on each cell — aggregate 4.0GB/s for maximum system
- ◇ 32 I/O links/ropes, 12-bit wide, 265MB/s (16 links/ropes on each cell) — 8.5GB/s I/O aggregate peak bandwidth
- ◇ 14 PCI-64/66 I/O buses for expansion slots
- ◇ Two PCI-64/33 I/O buses for expansion slots (for Core I/O SCSI/LAN)
- ◇ Two PCI-64/33 I/O buses for Core I/O (MP/SCSI)
- ◇ Two SCSI-3 Ultra160 LVD main storage I/O buses (one on each cell)
- ◇ Ultra SCSI SE for removable media (DVD/Tape)

Memory

- ◇ ECC DIMMs, low-voltage TTL interface, 125MHz frequency (traditional/PC-133 SDRAMs do not work)
- ◇ 256MB, 512MB and 1GB modules supported (2GB probably later too)
- ◇ 16 slots on each cell board (32 slots maximum in a full system configuration), installed in quads
- ◇ 32GB maximum (in a full system configuration with two cells)
- ◇ 64GB was given as maximum with “future” memory modules — probably working today

Expansion

There are in all 16 PCI 64-bit/66MHz slots in the I/O cage, which can be fully accessed when using a system with two cells — with one cell board only seven slots are available. One PCI slot is dedicated to the Core I/O card set (see above) so only 15 of the 16 PCI slots are available for expansion options.

- ◇ 14 “Twin-Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via two I/O links/ropes (aggregate 530MB/s), hot-plug capable
- ◇ Two “Turbo” PCI 64-bit/66MHz slots, each on an independent PCI bus, each connected via one I/O link/rope (265MB/s), hot-plug capable (one of these two Turbo slots is reserved for Core I/O LAN/SCSI)
- ◇ Twelve slots keyed for 3.3V (support either 3.3V or universal PCI cards)
- ◇ Four slots keyed for 5.0V (support either 5.0V or universal PCI cards)

Drives

- ✧ Four trays for low-profile 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector, hot-plug (two Core I/O card sets are needed to access all four drives)
- ✧ One tray for a half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external accessible

The two pairs of SCSI drives are each connected to a separate channel on one of the SCSI controllers of the Core I/O sets — for both pair of drives to work two Core I/O card sets are needed.

4.36.3 External connectors

- ✧ 68-pin VHDCI Ultra160 LVD external SCSI (external channel from LAN/SCSI board)
- ✧ Three DB9 male RS232C serial (local console, remote console, UPS) via a DB25 "M cable" (MP/SCSI board)
- ✧ 10/100Mbit Ethernet TP/RJ45 *Management LAN* (MP/SCSI board)
- ✧ Gigabit Ethernet TP/RJ45 (LAN/SCSI board)

4.36.4 ROM update

There is an firmware update available which contains the latest version version 6.5.

- ✧ `PF_CKEYMAT0605.txt`¹⁹⁵ has details about the contents and installation of the patch.
- ✧ `PF_CKEYMAT0605.tar.gz`¹⁹⁶ contains the patch.

4.36.5 References

Manuals

- ✧ User Guide `hp rp7405/7410 Servers`¹⁹⁷ (PDF) Hewlett-Packard Company (2002, third edition)

Articles

- ✧ *hp server rp7410 whitepaper*, Hewlett-Packard Company (March 2002, product number 5980-9997EN) [did not find an appropriate URL for this PDF document — *Ed.*]

4.36.6 Operating systems

- ✧ HP-UX: 11i (v1, v2 and v3) (11.00 unsure and officially unsupported)
- ✧ Linux: *should* work

¹⁹⁵http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0605.txt

¹⁹⁶http://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0605.tar.gz

¹⁹⁷<http://docs.hp.com/en/A6752-96008/A6752-96008.pdf>

4.36.7 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 <i>rate</i> , int	SPEC2000 <i>rate</i> , fp
N4000-7Xrp7410			4-CPU: 25.38-CPU:49.9	4-CPU: 18.98-CPU:36.8

4.36.8 Physical dimensions

- ◇ Rack-mounted: 10U height
- ◇ Up to two hot-swappable/redundant power supplies (one is standard)

4.37 HP 9000 rp3410 & rp3440

4.37.1 Overview

Time of introduction: 2004

The rp3400 series rp3410 and rp3440 servers are one of the last PA-RISC-based HP 9000 systems, either to be used rack-mounted (2U) or stand-alone. They are driven by dual-core PA-8800 *Mako* or PA-8900 processors. At the core of the system is HP's *zx1* chipset, also used with Itanium 2 processors. There is an upgrade path to Intel/HP IA64 Itanium 2 processors. The HP 9000 rp4410 and rp4440 servers are technically very similar with a large range of processing and expansion possibilities. However the rp3410/rp3440 are the little brothers of the rp44xos—they feature fewer processors, a smaller amount of memory, fewer expansion slots and onboard I/O controllers (only one Gigabit Ethernet and Ultra SCSI) and lesser memory and I/O bandwidth than those (however they have one more SCSI drive).

List price at time of introduction: US \$4,000 for a (single-CPU, dual-core) rp3410 and US \$7,000 for a (single-CPU, dual-core) rp3440.

4.37.2 Internals

CPU

rp3410

- ◇ Dual-core PA-8800 800MHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each

rp3440

- ◇ 1 or 2 dual-core PA-8800 900MHz-1.0GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each
- or
- ◇ 1 or 2 dual-core PA-8900 800MHz-1.1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 64MB off-chip L2 cache each

Notes

1. It is possible to upgrade the CPUs to Itanium 2/IA64 processors.
2. The minimum system configurations were shipped with one CPU *with one core disabled* which could be software-upgraded.

Chipset

The systems are based on HP's **zx1 chipset**, which consists of two main components—the **MIO** (memory and I/O controller) and the **IOAs** (I/O adapters). The **zx1** is very close to a crossbar chipset—the **zx1** memory controller acts as the crossbar switch which links processors, memory and I/O together.

- ◇ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:

1. Processor bus (6.4GB/s) for one (rp3410) or two (rp3440) CPUs
2. Two independent memory buses (each 4.25GB/s)
3. The I/O channels (via the IOAs, see below)—six on rp3410 (3.0GB/s) and eight on rp3440 (4.0GB/s)

The zx1 MIO also contains both memory and cache controllers.

The rp3410 and rp3440 have different I/O configurations based on IOAs:

- ◇ rp3410: Five **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.0GB/s on six 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on two channels—1.0GB/s
 2. PCI-X 64/133 I/O slot on one channel—0.5GB/s
 3. Management LAN and serial ports (iLO card) on one channel—0.5GB/s
 4. Ultra160 SCSI and Gigabit Ethernet controllers on one channel—0.5GB/s
 5. IDE and USB controllers one channel—0.5GB/s
- ◇ rp3440: Seven **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0GB/s on eight 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on two channels—1.0GB/s
 2. PCI-X 64/133 I/O slot on one channel—0.5GB/s
 3. PCI-X 64/133 I/O slot on one channel—0.5GB/s
 4. PCI-X 64/133 I/O slot on one channel—0.5GB/s
 5. Management LAN and serial ports (iLO card) on one channel—0.5GB/s
 6. Ultra160 SCSI and Gigabit Ethernet controllers on one channel—0.5GB/s
 7. IDE and USB controllers on one channel—0.5GB/s

The “I/O connectivity” part of the chipset is made up of standard third-party I/O chips:

- ◇ Dual-channel Ultra160 SCSI controller (LSI Logic 53C1030)
- ◇ Gigabit Ethernet controller (Broadcom Tigon 3)
- ◇ IDE controller (PCI649)
- ◇ USB2.0 controller

Buses

- ◇ Itanium 2/zx1 processor bus, 128-bit, 200MHz, 6.4GB/s
- ◇ Two independent zx1 memory buses, 266MHz, each 4.25GB/s—aggregate 8.5GB/s memory bandwidth
- ◇ rp3410:
 - Six zx1 I/O channels/buses, aggregate 3.0GB/s
 - Two PCI-X 64/133 I/O buses

- ◇ rp3440:
 - Eight ZX1 I/O channels/buses, aggregate 4.0GB/s
 - Four PCI-X 64/133 I/O buses
- ◇ SCSI-3 Ultra160 (LVD) storage I/O bus
- ◇ IDE secondary storage I/O bus

Memory

- ◇ PC2100 parity ECC DDR CL2 SDRAM DIMMs
- ◇ Twelve slots
- ◇ 1GB minimum memory (4×256MB)
- ◇ rp3410: 6GB maximum memory
- ◇ rp3440: 32GB maximum memory (with eight 4GB DIMMs—the other four slots must be left empty in this maximum configuration)
- ◇ 8.5GB/s memory bandwidth
- ◇ 80ns memory latency

Expansion

- ◇ One PCI-X 64-bit/133MHz slot (1GB/s sustained data rate)
- ◇ rp3410: One PCI-X 64-bit/133MHz slot (512MB/s sustained data rate)
- ◇ rp3440: Three PCI-X 64-bit/133MHz slots (512MB/s sustained data rate)
- ◇ (rp3410 has overall two slots, rp3440 four slots)
- ◇ All PCI slots are 3.3V

Drives

- ◇ Three bays for 3.5" Ultra160 LVD SCSI hard drives, 1" height, 68-pin
- ◇ Slimline bay for optional IDE CD or DVD drive

4.37.3 External connectors

- ◇ Three DB9 male RS232C serial (local console, remote console, general purpose)
- ◇ Four USB 2.0 ports
- ◇ TP/RJ45 Gigabit Ethernet
- ◇ HP Integrated Lights Out (iLO) system management card with Fast-Ethernet Web console
- ◇ Ultra160 SCSI 68-pin

4.37.4 References

Manuals

- ◇ User Service Guide HP 9000 rp3410 and HP 9000 rp3440¹⁹⁸ (PDF) Hewlett-Packard Development Company (April 2007, fourth edition)
- ◇ Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers¹⁹⁹ (PDF, 700KB) Hewlett-Packard (2005)

4.37.5 Operating systems

- ◇ HP-UX: 11i v1, v2 or v3 (foundation, enterprise or MCOE or TCOE)
- ◇ Linux seems to be supported on at least the rp3440 (according to ESIEE)

4.37.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 rate, int	SPEC2000 rate, fp
rp3440 1.0GHz dualcore			2-core: 18.7 2-CPU/4-core: 37.1	2-core: 19.2 2-CPU/4-core: 32.6

4.37.7 Physical dimensions/Power

- ◇ Rack-mounted: 2U height, 483×680 mm width/depth
- ◇ Vertical stand-alone: 495×295×675 mm height/width/depth
- ◇ Weight of 23-26kg stand-alone, 18-23kg rack-mounted
- ◇ Typical power consumption of 600W
- ◇ One or two hot-swap power-supplies (one is standard)

¹⁹⁸<http://docs.hp.com/en/A7137-96008/A7137-96008.pdf>

¹⁹⁹<http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf>

4.38 HP 9000 rp4410 & rp4440

4.38.1 Overview

Time of introduction: 2004

The rp4400 series rp4410 and rp4440 servers are, as their smaller rp3410 and rp3440 siblings, one of the last PA-RISC-based HP servers. They are driven by up to two (rp4410) or four (rp4440) dual-core PA-8800 *Mako* or PA-8900 processors. The rp4400s are based around the Itanium 2/IA64-capable HP *zx1* chipset, and technically very similar to the rp3400's architecture. The systems can be rack-mounted (4U) or used stand-alone.

List price at time of introduction: US \$21,000 for a (single-CPU, dual-core) rp4440.

4.38.2 Internals

CPU

rp4410

- ◇ 1 or 2 dual-core PA-8800 900MHz-1.0GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each
- or
- ◇ 1 or 2 dual-core PA-8900 800MHz-1.1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 64MB off-chip L2 cache each

rp4440

- ◇ 1, 2 or 4 dual-core PA-8800 900MHz-1.0GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each
- or
- ◇ 1, 2 or 4 dual-core PA-8900 800MHz-1.1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 64MB off-chip L2 cache each

It is probably possible to upgrade the CPUs to Itanium 2/IA64 processors.

Chipset

The systems are based on HP's **zx1 chipset**, which consists of three main components — the **MIO** (memory and I/O controller), the **IOAs** (I/O adapters) and the **SMEs** (scalable memory expanders):

- ◇ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:
 1. Processor bus (6.4GB/s) for one (rp4410) or two (rp4440) dual-CPU modules
 2. Two independent memory buses (each 6.4GB/s)
 3. Eight I/O channels (aggregate 4.0GB/s, via the IOAs, see below)

The **zx1 MIO** also contains both memory and cache controllers.

- ◇ Six **zx1 SMEs** (scalable memory expanders) attach to two independent **zx1** memory buses (each 6.4GB/s)
- ◇ Six **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the **zx1** MIO with an aggregate bandwidth of 4.0GB/s on eight 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 3. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 4. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 5. Core I/O adapters (SCSI, Ethernet etc.) on two channels — 1.0GB/s (one channel to dual-port Gigabit Ethernet and Ultra320 SCSI controller, one channel to the management LAN, serial and USB2.0 ports)

The “I/O connectivity” part of the chipset is made up of standard third-party I/O chips:

- ◇ Dual-channel Ultra320 SCSI controller
- ◇ Dual-port Gigabit Ethernet
- ◇ USB2.0 controller
- ◇ IDE controller

An interesting aspect of the rp4400’s bus setup is that the same 6.4GB/s processor bus is shared between up to two CPUs on the rp4410 and up to four CPUs on the rp4440.

Buses

- ◇ Itanium 2/zx1 processor bus 6.4GB/s
- ◇ Two independent **zx1** memory buses, 200MHz, each 6.4GB/s
- ◇ Eight **zx1** I/O channels/buses, aggregate 4.0GB/s
- ◇ Two PCI-X 64/133 I/O buses
- ◇ Two PCI-X 64/66 I/O buses
- ◇ SCSI-3 Ultra320 (LVD) storage I/O bus
- ◇ IDE secondary storage I/O bus

Memory

- ◇ PC2100 parity ECC DDR CL2 SDRAM DIMMs
- ◇ 16- or 32-DIMM carrier board
- ◇ 1GB minimum memory
- ◇ 128GB maximum memory
- ◇ 12.8GB/s memory bandwidth
- ◇ 105ns memory latency

Expansion

- ◇ Two PCI-X 64-bit/133MHz slots (each on an independent bus), hot-plug
- ◇ Four PCI-X 64-bit/66MHz slot (on two shared buses), hot-plug
- ◇ All PCI slots are 3.3V

Drives

- ◇ Two bays for 3.5" Ultra320 LVD SCSI hard drives, hot-plug
- ◇ Slimline bay for optional IDE CD or DVD drive

4.38.3 External connectors

- ◇ Three DB9 male RS232C serial (local console, remote console, general purpose)
- ◇ Two USB 2.0 ports
- ◇ Two Gigabit Ethernet, TP/RJ45
- ◇ Two Ultra320 SCSI ports
- ◇ HP Integrated Lights Out (iLO) system management card with Fast-Ethernet Web console

4.38.4 References

Manuals

- ◇ **User Service Guide HP 9000 rp4410 and HP 9000 rp4440²⁰⁰** (PDF) Hewlett-Packard Development Company (April 2007, third edition)
- ◇ **Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers²⁰¹** (PDF, 700KB) Hewlett-Packard (2005)

4.38.5 Operating systems

- ◇ HP-UX: 11i v1, v2 or v3 (foundation, enterprise or MCOE or TCOE)
- ◇ Linux could be a possibility, as the similar rp3400s are supported, albeit unofficially

4.38.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 <i>rate, int</i>	SPEC2000 <i>rate, fp</i>
rp4440 1.0GHz dualcore			2-core: 18.6 2-CPU/4-core: 37.0 4-CPU/8-core: 73.2	2-core: 19.3 2-CPU/4-core: 34.7 4-CPU/8-core: 55.4

²⁰⁰<http://docs.hp.com/en/A9950-96011/A9950-96011.pdf>

²⁰¹<http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf>

4.38.7 Physical dimensions/Power

- ◇ Rack-mounted: 4U height, 440×690 mm width/depth
- ◇ Vertical stand-alone: 530×261×695 mm height/width/depth
- ◇ Weight of maximum 51.53kg
- ◇ Typical power consumption of 836W (rp4410) or 1186W (rp4440)
- ◇ One or two hot-swap power-supplies (one is standard)

4.39 HP Integrity rx1600 & rx1620

4.39.1 Overview

The rx1600 (later rx1600-2) is a 1U rack-mountable server with up to two Itanium 2 Deerfield processors. The later introduced rx1620 supports newer Fanwood Itanium 2 processors. Both classes of CPUs are specified/marketed as “low-voltage.”

Time of introduction: 2004 (rx1600)/December 2004 (rx1620, with prices at the time starting at under \$3,000 (rx1600)/\$4,000 (rx1620).

4.39.2 Internals

CPU

rx1600/rx1600-2

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 <i>Deerfield</i> low-voltage	1.0GHz	16/16KB	256KB	1.5MB

rx1620

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 <i>Fanwood</i> low-voltage	1.3GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Fanwood</i> low-voltage	1.6GHz	16/16KB	256KB	3.0MB

All caches are on-die (L1, L2 and L3).

Chipset

The systems are based on HP's **zx1 chipset**, which consists of two main components — the **MIO** (memory and I/O controller) and the **IOAs** (I/O adapters):

- ◇ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:

1. Processor bus (6.4GB/s on 1.0 and 1.3GHz processors, 8.5GB/s on 1.6GHz processors)
2. Two independent memory buses (each 4.25GB/s)
3. Seven I/O channels (aggregate 3.5GB/s, via the IOAs, see below)

The zx1 MIO also contains both memory and cache controllers.

- ◇ Five **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.5GB/s on seven 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 3. Gigabit Ethernet and Ultra320 SCSI (Core I/O) on PCI on one channel — 0.5GB/s
 4. IDE, USB, Fast-Ethernet LAN (Core I/O) on PCI on one channel — 0.5GB/s

5. Management Ethernet LAN, VGA, serial (Core I/O) on PCI on one channel — 0.5GB/s

The “I/O connectivity” part of the chipset is made up of standard third-party I/O chips:

- ✧ Gigabit Ethernet (Broadcom 5701)
- ✧ rx1600: Fast Ethernet
- ✧ Two-channel Ultra320 SCSI controller (LSI 53C1030)
- ✧ Ultra ATA-100 IDE controller (PCI649)
- ✧ Serial controller, DUART (16550A-compatible)
- ✧ 10/100 Ethernet for management (Intel 82550)
- ✧ Management processor card included by default
- ✧ Processor Dependent Hardware (PDH) Controller
- ✧ FPGA controller for ACPI (2.0) and LPC
- ✧ Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)
- ✧ EHCI USB controller

Buses

- ✧ Itanium 2/ZX1 processor bus — 200MHz DDR with 6.4GB/s bandwidth on 1.0 and 1.3GHz processors, 266MHz DDR with 8.5GB/s on 1.6GHz processors (rx1620)
- ✧ Two independent ZX1 memory buses, 266MHz, each 4.25GB/s — aggregate 8.5GB/s memory bandwidth
- ✧ Seven ZX1 I/O channels/buses, aggregate 3.5GB/s
- ✧ Four PCI-X 64/133 I/O buses for expansion cards
- ✧ Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- ✧ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ✧ UltraATA-100 IDE storage I/O bus

Memory

- ✧ PC2100 ECC DDR CL2 SDRAM DIMMs
- ✧ Takes up to 2GB modules
- ✧ Eight slots
- ✧ DIMMs must be installed in quads
- ✧ 1GB minimum (4×256MB)
- ✧ 16GB maximum (8×2GB)
- ✧ 8.5GB/s memory bandwidth

Expansion

- ◇ PCI-X 64-bit/133MHz slot, full-length
- ◇ PCI-X 64-bit/133MHz slot, half-length
- ◇ All PCI slots are 3.3V

Drives

- ◇ Two internal 3.5" bays for 1" height Ultra320 SCSI SCA 80-pin hard drives, hot-plug; drives 1 and 2 are on one SCSI channel, drive 3 on the second SCSI channel
- ◇ Slimline bay for optional IDE CD or DVD drive

4.39.3 External connectors

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ rx1600: 10/100 Ethernet, TP/RJ45
- ◇ rx1620: Second Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Ultra320 SCSI 68-pin HDCL
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Two USB 2.0 ports
- ◇ Two DB9 male RS232C serial

4.39.4 References

Manuals

- ◇ **hp Integrity rx1600 Operation and Maintenance**²⁰² (PDF) Hewlett-Packard Development Company (January 2004)
- ◇ **hp Integrity rx1620 Operations Guide**²⁰³ (PDF) Hewlett-Packard Development Company (February 2005, AB430-96005)
- ◇ **hp Integrity rx1620 Maintenance Guide**²⁰⁴ (PDF) Hewlett-Packard Development Company (February 2005, AB430-96006)

²⁰²<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404636/co1404636.pdf>

²⁰³<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404664/co1404664.pdf>

²⁰⁴<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404656/co1404656.pdf>

Articles

- ◇ Overview of the HP Integrity rx1600, rx2600, rx4640, and rx5670 servers technical whitepaper²⁰⁵ (PDF) Hewlett-Packard Development Company (January 2004, second edition, 5982-1595EN)
- ◇ Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers²⁰⁶ (PDF) Hewlett-Packard Development Company (December 2006, rev. 4, 5982-9835EN)

4.39.5 Operating systems

- ◇ HP-UX 11i v2 and v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

4.39.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
rx1600 1.0GHz 1.5MB	837	1382	9.71 2-CPU: 19.1	16.0 2-CPU: 27.6
rx1620-21.3GHz 3.0MB	1178	2214	13.7 2-CPU: 27.0	25.7 2-CPU: 42.7
rx1620-21.6GHz 3.0MB	1452	2692	16.8 2-CPU: 33.2	31.2 2-CPU: 50.4

4.39.7 Physical dimensions/Power

- ◇ 1U (rack-mount) height, 482×680 mm width/depth
- ◇ 17.5kg net weight, 22.2kg fully loaded
- ◇ rx1600: 400W power supply
- ◇ rx1620: 460W power supply

²⁰⁵http://www.nitrosystem.com/pdf/rx_servers_wp_01-23-04.pdf

²⁰⁶<http://h71028.www7.hp.com/ERC/downloads/5982-9835EN.pdf>

4.40 HP Integrity rx2600 & rx2620

4.40.1 Overview

The rx2600 is the rack-designated sibling of the zx6000 workstation. They feature a very similar system design and casing and can be both mounted in 2U of a 19" rack. Also based on one or two Itanium 2 processors the rx2600 architecture differs from the zx6000 in that it is targeted for PCI-X I/O devices and thus does not feature the AGP port of the workstation-oriented zx6000.

The rx2600 was later marketed as **rx2600-2**.

Time of introduction: 2002-2003 (rx2600)/December 2004 (rx2620) with prices at the time starting at \$7,300 (entry rx2600), \$16,000 (average rx2600) to \$33,000 (large rx2600).

4.40.2 Internals

CPU

rx2600/rx2600-2

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 <i>Deerfield</i> ? low-voltage	1.0GHz	16/16KB	256KB	1.5MB
1-2	Itanium 2 <i>Madison</i>	1.3GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Madison</i>	1.4GHz	16/16KB	256KB	1.5MB
1-2	Itanium 2 <i>Madison</i>	1.5GHz	16/16KB	256KB	6.0MB

rx2620

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 <i>Madison</i> ?	1.3GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Madison</i> ?	1.6GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Montecito</i> dual-core	1.4GHz	16/16KB	1024/256KB	12MB
1-2	Itanium 2 <i>Montecito</i> dual-core	1.6GHz	16/16KB	1024/256KB	18MB

All caches are on-die (L1, L2 and L3).

Chipset

The systems are based on HP's **zx1 chipset**, which consists of two main components—the **MIO** (memory and I/O controller) and the **IOAs** (I/O adapters):

◇ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:

1. Processor bus (6.4GB/s at 200MHz DDR)
2. Two independent memory buses (each 4.25GB/s)
3. Eight I/O channels (aggregate 4.0GB/s, via the IOAs, see below)

The **zx1 MIO** also contains both memory and cache controllers.

◇ Seven **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the **zx1 MIO** with an aggregate bandwidth of 4.0GB/s on eight 0.5GB/s channels

1. PCI-X 64/133 I/O slot on two channels—1.0GB/s
2. PCI-X 64/133 I/O slot on one channel—0.5GB/s
3. PCI-X 64/133 I/O slot on one channel—0.5GB/s
4. PCI-X 64/133 I/O slot on one channel—0.5GB/s
5. Core I/O: IDE, USB, serial, (rx2600 only: Fast-Ethernet LAN) in a PCI 64/133 slot on one channel—0.5GB/s
6. Core I/O: Gigabit Ethernet and Ultra320 SCSI (on rx2620 there are each two Gigabit Ethernet and SCSI controllers) in a PCI 64/133 slot on one channel—0.5GB/s
7. Management: Ethernet LAN, VGA, serial in a PCI 64/133 slot on one channel—0.5GB/s

The “I/O connectivity” part of the chipset is made up of standard third-party I/O chips:

- ✧ Gigabit Ethernet (Broadcom 5701)
- ✧ Two-channel Ultra320 SCSI controller (LSI 53C1030)
- ✧ Ultra ATA-100 IDE controller (PCI649)
- ✧ Serial controller, DUART (16550A-compatible)
- ✧ 10/100 Ethernet for management (Intel 82550)
- ✧ Management processor card included by default (“ECI card”)—includes serial/ remote management and VGA
- ✧ Radeon VGA graphics
- ✧ EHCI USB controller
- ✧ Processor Dependent Hardware (PDH) Controller
- ✧ FPGA controller for ACPI (2.0) and LPC
- ✧ Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)

Buses

- ✧ Itanium 2/zx1 processor bus 6.4GB/s at 200MHz DDR
- ✧ Two independent zx1 memory buses, 266MHz, each 4.25GB/s—aggregate 8.5GB/s memory bandwidth
- ✧ Eight zx1 I/O channels/buses, aggregate 4.0GB/s
- ✧ Four PCI-X 64/133 I/O buses for expansion cards
- ✧ Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- ✧ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ✧ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 ECC DDR CL2 SDRAM DIMMs
- ◇ rx2600: up to 2GB modules
- ◇ rx2620: up to 4GB modules
- ◇ Twelve slots
- ◇ DIMMs must be installed in quads
- ◇ 1GB minimum (4×256MB)
- ◇ rx2600: 24GB maximum (12×2GB)
- ◇ rx2620: 32GB maximum (8×4GB—the remaining four slots cannot be used)
- ◇ 8.5GB/s memory bandwidth

Expansion

- ◇ Four PCI-X 64-bit/133MHz slots, full-length
- ◇ All PCI slots are 3.3V

Drives

- ◇ Three internal 3.5" bays for Ultra320 SCSI SCA 80-pin hard drives, hot-plug; drives 1 and 2 are on one SCSI channel, drive 3 on the second SCSI channel
- ◇ Slimline bay for optional IDE CD or DVD drive

4.40.3 External connectors

- ◇ rx2600: Gigabit Ethernet, TP/RJ45
- ◇ rx2620: Dual-Port Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Four USB 2.0 ports
- ◇ Two DB9 male RS232C serial

4.40.4 References

Manuals

- ◇ **Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000**²⁰⁷ (PDF) Hewlett-Packard Development Company (September 2003, second edition)
- ◇ **User Service Guide HP Integrity rx2620 Server**²⁰⁸ (PDF) Hewlett-Packard Development Company (August 2006, first edition, AD117-9003A)

Articles

- ◇ **Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers**²⁰⁹ (PDF) Hewlett-Packard Development Company (December 2006, rev. 4, 5982-9835EN)
- ◇ **Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper**²¹⁰ (PDF) Hewlett-Packard Development Company (October 2003, first edition, 5982-1595EN)

4.40.5 Operating systems

- ◇ rx2600: HP-UX 11i v1.6, v2 and v3
- ◇ rx2620: HP-UX 11i v2 and v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

4.40.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
rx2600 900MHz 1.5MB	674	1151	7.8 2-CPU: 15.5	2-CPU:
rx2600 1.0GHz 3.0MB	810	1427	9.4 2-CPU: 18.7	2-CPU:
rx2600 1.3GHz 3.0MB	1073	1808	12.4 2-CPU: 24.8	2-CPU:
rx2600 1.5GHz 6.0MB	1408	2119	15.3 2-CPU: 30.5	2-CPU:
rx2620-2 1.3Hz 3.0MB	1170	2229	13.6 2-CPU: 26.9	15.9 2-CPU: 27.7
rx2620-2 1.6Hz 3.0MB	1408	2553	16.3 2-CPU: 32.3	29.6 2-CPU: 48.5
rx2620-2 1.6Hz 6.0MB	1535	2675	17.8 2-CPU: 35.5	31.0 2-CPU: 51.5

4.40.7 Physical dimensions/Power

- ◇ Tower: 495×297×673 mm height/width/depth
- ◇ Tower: 22kg net weight, 25.5kg fully loaded
- ◇ Rack-mounted: 2U height, 482×680 mm width/depth

²⁰⁷<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpno4096/lpno4096.pdf>

²⁰⁸<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404139/co1404139.pdf>

²⁰⁹<http://h71028.www7.hp.com/ERC/downloads/5982-9835EN.pdf>

²¹⁰http://www.hpsystem.com/pdf/10420_rx2600_rx4640_rx5670_wp_102303.pdf

- ◇ Rack-mounted: 17.5kg net weight, 22kg fully loaded
- ◇ There exists a kit for converting the rack-mount version into a pedestal/tower one, which includes removing the rack rails and changing the fan/cooling system
- ◇ 650W hot-swap power supplies (one standard, optional second)

4.4.1 HP Integrity rx4610

4.4.1.1 Overview

The Integrity rx4610 were HP's first-generation Itanium server based on up to four *Merced* Itanium processors and integrated into an 7U rack-mountable case. The rx4610 offered many I/O and expansion options with ten PCI slots on four PCI buses (attached to 2.1GB/s of I/O bandwidth) and up to 64GB of main memory but was limited to only two internal SCSI drives.

The rx4610 is based on the Intel Itanium reference architecture—the 82460GX chipset, which looks like a mix of PC-style (Frontside Bus to the processor) and PA-RISC (I/O “ropes” from the central chipset to PCI converters) platforms. The other HP system with Merced processors and the 82460GX was the HP i2000 workstation. Both the i2000 and rx4610 were rather slow and buggy when compared to contemporary PA-RISC systems.

Time of introduction: 2001, discontinued: Fall 2002, with prices at time of introduction between \$25,000 (733MHz base system)/\$37,000 (800MHz base system) to more than \$45,000 (larger systems).

4.4.1.2 Internals

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
2-4	Itanium 1 <i>Merced</i>	733MHz	16/16KB	96KB	2.0MB
2-4	Itanium 1 <i>Merced</i>	800MHz	16/16KB	96KB	4.0MB

L1 and L2 caches are on-die, L3 is off-chip

Chipset

The rx4610 is based on Intel's 82460GX chipset with four main components:

1. **82460GX SAC** (System Address Chip) is the central chipset part:

- ✧ System bus (FSB) for up to four processors—2.1GB/s (the SAC connects to the address and control parts of the FSB)
- ✧ Four I/O channels to which the PCI buses attach (via the WXBs/PXB)—each channel is 533MB/s
- ✧ Connection to the SDC
- ✧ Address/control access to the main memory

2. Three **82460GX WXBs** (Wide eXpansion Bridges) which connect the PCI 64/66 buses via three I/O channels to the SAC

- ✧ One I/O channel connects to two PCI 64/66 slots
- ✧ One I/O channel connects to three PCI 64/66 slots
- ✧ One I/O channel connects to three PCI 64/66 slots and the SCSI controller

3. **82460GX PXB** (PCI eXpansion Bridge) connects the PCI 64/33 bus and core I/O (Ethernet LAN, PS/2, parallel, serial, IDE, USB, VGA) and the baseboard management controller via one I/O channel to the SAC
4. **82460GX SDC** (System Data Chip) is the central memory data controller:
 - ✧ It connects to the data part of the FSB system main bus
 - ✧ Has a private link to the SAC (PD)
 - ✧ Connects to the memory subsystem (data transfers, in contrast to the SAC's Address/control access)

The rest of the chipset is made up of standard (third-party) I/O components:

- ✧ Dual-channel Ultra3 SCSI controller
- ✧ Intel 82559 Fast Ethernet controller
- ✧ ATI Rage 128VR 64-bit SVGA with 16MB video memory
- ✧ Baseboard management controller (BMC) for IPMI, EMP and WoL
- ✧ I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- ✧ ATA-33 IDE controller (on IFB)
- ✧ USB controller (on IFB)
- ✧ LPC47B27 Super I/O (serial and PS/2 ports controller)

Buses

- ✧ System bus, 32bit 133MHz DDR (“double-pumped”), 2.1GB/s, ECC-protected
- ✧ Memory bus, 266MHz, 4.2GB/s peak
- ✧ 2.1GB/s aggregate I/O bandwidth with four 533MB/s I/O channels
- ✧ Three PCI 64/66 I/O buses for expansion slots
- ✧ PCI 64/33 I/O bus for expansion slots and onboard devices

Memory

- ✧ Two memory boards, each supports up to 32GB of memory
- ✧ 72-bit DIMMs
- ✧ 32 slots on each memory board
- ✧ Up to 1GB modules
- ✧ 1GB minimum (*i.e.*, one board)
- ✧ 64GB maximum (64×1GB—32 modules on two boards)

Expansion

- ◇ Eight PCI 64-bit/66MHz slots, full-length, hot-plug, 3.3V
 - Two slots are on one I/O channel
 - Three slots are on one I/O channel
 - Three slots are on one I/O channel which is shared with the SCSI subsystem
- ◇ Two PCI 64-bit/33MHz slots, full-length, 5.0V

Drives

- ◇ Two internal 3.5" bays for 1" height LVD SCA2 SCSI hard drives
- ◇ Optional IDE DVD drive in 0.5" carrier
- ◇ Optional IDE floppy drive (LS120) in 0.5" carrier

4.41.3 External connectors

- ◇ 10/100 Ethernet, TP/RJ45
- ◇ VGA graphics
- ◇ External SCSI
- ◇ Two PS/2 for keyboard and mouse
- ◇ Parallel port
- ◇ Two 9-pin serial
- ◇ Two USB

4.41.4 References

Manuals

- ◇ **hp server rx4610 User Guide**²¹¹ (PDF) Hewlett-Packard Company (n. d., version 0501)

Articles

- ◇ *An overview of the Itanium-based hp rx4610 server whitepaper*, Hewlett-Packard Company (June 2001, product number 5980-6420EN) [did not find an appropriate URL for this PDF document —Ed.]

²¹¹<http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00112381/c00112381.pdf>

4.41.5 Operating systems

- ◇ HP-UX 11i v1.5
- ◇ Linux for Itanium
- ◇ Windows 64-bit

4.41.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
rx4610733MHz 2MB		625		7.22-CPU: 12.74-CPU: 20.1
rx4610800MHz 4MB	379	701	4.4	8.12-CPU: 14.24-CPU: 22.4

4.41.7 Physical dimensions/Power

- ◇ 7U (rack-mount) height, 444×711 mm width/depth
- ◇ 68.1 kg max weight
- ◇ Four 800W power supplies, minimum of three required (N+1)

4.42 HP Integrity rx4640

4.42.1 Overview

The Integrity rx4640 (rx4640-8) are second-generation Itanium servers from HP with up to four Itanium 2 processors in a 4U rack-mountable case. In contrast to the rx4610 predecessors (7U, first-generation Itanium) the rx4640 is a completely new design based on the HP zx1 Itanium chipset, with double the I/O bandwidth and three times the processor and memory bandwidth. The rx4640 features a large amount of maximum memory (128GB) but fewer PCI slots (six) and only the same small number of two internal SCSI drives.

The rx4640 was later marketed as **rx4640-8**.

Time of introduction: December 2004 with prices at time of introduction starting at \$15,000.

4.42.2 Internals

CPU

The “standard” rx4640 supported out of the box up to four Itanium 2 processors:

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3	Other
1-4	Itanium 2 <i>Madison</i>	1.3GHz	16/16KB	256KB	3.0MB	
1-4	Itanium 2 <i>Madison</i>	1.5GHz	16/16KB	256KB	6.0MB	

Later rx4640 models (probably with a firmware upgrade) supported various newer processors, including dual-core Montvale CPUs and the **mx2** dual-CPU modules.

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3	Other
1-4	Itanium 2 <i>Madison</i>	1.6GHz	16/16KB	256KB	6.0MB	
1-4	Itanium 2 <i>Madison</i>	1.6GHz	16/16KB	256KB	9.0MB	
1-4	Itanium 2 <i>Montvale</i> dual-core (9140N)	1.6GHz	16/16KB	1024/256KB	18MB	
1-4	Itanium 2 <i>Montvale</i> dual-core (9150N)	1.6GHz	16/16KB	1024/256KB	24MB	
1-4	Itanium 2 mx2 <i>Hondodual-CPU</i> module	1.1GHz	16/16KB	256KB	4.0MB	32MB L4

Chipset

The rx4640 are based on HP’s **zx1 chipset**, which consists of three main components — the **MIO** (memory and I/O controller), the **IOAs** (I/O adapters) and the **SMEs** (scalable memory expanders):

✧ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:

1. Processor bus (6.4GB/s at 200MHz DDR)
2. Two independent memory buses (each 6.4GB/s)
3. Eight I/O channels (aggregate 4.0GB/s, via the IOAs, see below)

The **zx1 MIO** also contains both memory and cache controllers.

✧ Six **zx1 SMEs** (scalable memory expanders) attach to two independent **zx1** memory buses (each 6.4GB/s with three SMEs)

- ◇ Six **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the **zx1 MIO** with an aggregate bandwidth of 4.0GB/s on eight 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 3. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 4. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 5. Core I/O: SCSI and Gigabit Ethernet on one channel — 0.5GB/s
 6. Core I/O: Management LAN, IDE, USB, serial and VGA on one channel — 0.5GB/s

The I/O connectivity part of the chipset is made up of standard third-party I/O chips:

- ◇ Gigabit Ethernet (Broadcom 5701)
- ◇ Two-channel Ultra320 SCSI controller (LSI 53C1030)
- ◇ Ultra ATA-100 IDE controller (PCI649)
- ◇ EHCI USB controller
- ◇ Serial controller, DUART (16550A-compatible)
- ◇ “Diva” remote management processor — serial and LAN
- ◇ Processor Dependent Hardware (PDH) Controller
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)

Buses

- ◇ Itanium 2/zx1 processor bus 6.4GB/s at 200MHz DDR
- ◇ Two independent **zx1** memory buses, 200MHz, each 6.4GB/s — aggregate 12.8GB/s memory bandwidth
- ◇ Eight **zx1** I/O channels/buses, aggregate 4.0GB/s
- ◇ Two PCI-X 64/133 I/O buses
- ◇ Two PCI-X 64/66 I/O buses
- ◇ PCI-X 64/66 I/O bus (for SCSI/Gigabit Ethernet onboard)
- ◇ PCI 32/33 I/O bus (for IDE/USB/management onboard devices)
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ DDR200 CL2 registered ECC SDRAM DIMMs, 200MHz, 184-pin 2.5V

- ◇ Takes up to 4GB modules
- ◇ 16-DIMM or 32-DIMM memory carrier board
- ◇ DIMMs must be installed in quads
- ◇ 1GB minimum (4×256MB)
- ◇ 64GB maximum with 16-DIMM board (16×2GB), 128GB maximum with 32-DIMM board (32×4GB)
- ◇ 12.8GB/s memory bandwidth

Expansion

- ◇ Four PCI-X 64-bit/66MHz slots, hot-plug. 3.3 V
- ◇ Two PCI-X 64-bit/133MHz slots, hot-plug. 3.3 V

Drives

- ◇ Two internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug; each drive can be configured on one separate channel—if they are on the same channel the second can be used for external SCSI devices
- ◇ Slimline bay for optional IDE CD or DVD drive

4.42.3 External connectors

- ◇ Dual-port Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Two external Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Four USB 2.0 ports
- ◇ Two (three?) DB9 male RS232C serial

4.42.4 References

Manuals

- ◇ **User Service Guide HP Integrity rx4640 Server²¹²** (PDF) Hewlett-Packard Development Company (August 2006, first edition, A6961-96013)

²¹²<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/c01404141/c01404141.pdf>

Articles

- ◇ Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers²¹³ (PDF) Hewlett-Packard Development Company (December 2006, rev. 4, 5982-9835EN)
- ◇ Overview of the HP Integrity rx1600-2, rx2600-2, and rx4640-8 servers technical whitepaper²¹⁴ (PDF) Hewlett-Packard Development Company (April 2004, 5982-5031EN)
- ◇ Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper²¹⁵ (PDF) Hewlett-Packard Development Company (October 2003, first edition, 5982-1595EN)

4.42.5 Operating systems

- ◇ HP-UX 11i v2 and v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

4.42.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 rate, int	SPEC2000 rate, fp
rx4640 1.3GHz 3.0MB	1132	1891	13.1 2-CPU: 25.8 4-CPU: 51.4	21.9 2-CPU: 37.9 4-CPU: 57.4
rx4640 1.5GHz 6.0MB	1404	2161	16.3 2-CPU: 32.5 4-CPU: 64.2	25.1 2-CPU: 43.2 4-CPU: 65.6
rx4640-8 1.5GHz 4.0MB	1372	2502	15.9 2-CPU: 31.7 4-CPU: 62.2	29 2-CPU: 48.3 4-CPU: 70.5
rx4640-8 1.6GHz 9MB	1590	2712	4-CPU: 72.5	4-CPU: 77.9

4.42.7 Physical dimensions/Power

- ◇ 4U height, 482×690 mm width/depth
- ◇ 40kg net weight, 45kg fully loaded
- ◇ 650/1200W hot-swap power supplies (one standard, optional second)

²¹³ <http://h71028.www7.hp.com/ERC/downloads/5982-9835EN.pdf>

²¹⁴ http://h71028.www7.hp.com/ERC/downloads/rx4640_2600_1600_wp_FINAL_4-14-04.pdf

²¹⁵ http://www.hpsystem.com/pdf/10420_rx2600_rx4640_rx5670_wp_102303.pdf

4.43 HP Integrity rx5670

4.43.1 Overview

The rx5670 is a 7U rack-mountable SMP Itanium 2 server with up to four processors. Closely matching the rx4640 system architecture, the rx5670 is based on HP's zx1 Itanium chipset. PA-RISC L-Class servers (built into the same system/chassis) could be upgraded by a “board-swap” — changing the main system board, processors and support hardware — to Itanium 2 rx5670s (applies to HP rp5400/rp5450 (L1000/L2000) and HP rp5430/rp5470 (L1500/L3000)).

Time of introduction: 2002-2003, with prices at time of introduction between \$23,000 (entry), \$38,000 (average), \$64,000 (large).

4.43.2 Internals

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-4	Itanium 2 <i>Madison</i>	1.3GHz	16/16KB	256KB	3.0MB
1-4	Itanium 2 <i>Madison</i>	1.3GHz	16/16KB	256KB	6.0MB

All caches are on-die (L1, L2 and L3).

Chipset

The rx5670 is based on HP's **zx1 chipset**, which consists of three main components — the **MIO** (memory and I/O controller), the **IOAs** (I/O adapters) and the **SMEs** (scalable memory expanders):

- ◇ **zx1 MIO** (memory and I/O controller) is the main chipset controller and connects the three central system buses:

1. Processor bus (6.4GB/s at 200MHz DDR)
2. Two independent memory buses (each 6.4GB/s with six SMEs)
3. Eight I/O channels (aggregate 4.0GB/s, via the IOAs, see below)

The zx1 MIO also contains both memory and cache controllers.

- ◇ Twelve **zx1 SMEs** (scalable memory expanders), six on each DIMM/memory carrier board, attach to two independent zx1 memory buses (each 6.4GB/s)
- ◇ Eight **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0GB/s on eight 0.5GB/s channels
 1. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 2. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 3. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 4. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 5. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s

6. Two PCI-X 64/66 I/O slots on one channel — 0.5GB/s
7. One PCI 64/66 slot for Gigabit Ethernet and one SCSI controller (Core I/O) on one channel — 0.5GB/s
8. One PCI 64/66 slot for management LAN, serial and one SCSI controller (Core I/O); and one PCI 64/33 slot for optional graphics/USB on one channel (with the other slot) — 0.5GB/s

The I/O connectivity part of the chipset is made up of standard third-party I/O chips, implemented on Core I/O cards in two or three PCI slots

- ✧ Dual-channel Ultra160 SCSI controllers (LSI 53C1010)
- ✧ SCSI controller (LSI 53C896)
- ✧ Gigabit Ethernet (Broadcom 5701)
- ✧ Serial controller, DUART (16550A-compatible)
- ✧ IBM PCI-X to PCI-X bridge
- ✧ “Diva” remote management processor—serial and LAN
- ✧ Optional Radeon VGA graphics (with USB on one card)
- ✧ Optional EHCI USB controller

Buses

- ✧ Itanium 2/zx1 processor bus 6.4GB/s at 200MHz DDR
- ✧ Two independent zx1 memory buses, 266MHz, each 6.4GB/s—aggregate 12.8GB/s memory bandwidth
- ✧ Eight zx1 I/O channels/buses, aggregate 4.0GB/s
- ✧ Three PCI-X 64/133 I/O buses for expansion slots
- ✧ Three PCI-X 64/66 I/O buses for expansion slots
- ✧ PCI-X 64/66 I/O bus for Core I/O expansion slots
- ✧ PCI 64/33 I/O bus for graphics/USB slot
- ✧ Two SCSI-3 Ultra160 (LVD) storage I/O buses

Memory

- ✧ PC2100 ECC DDR CL2 SDRAM DIMMs
- ✧ Takes up to 2GB modules
- ✧ One or two 24-DIMM memory carrier boards
- ✧ DIMMs must be installed in quads
- ✧ 1GB minimum (4×256MB)
- ✧ 96GB maximum with two 24-DIMM boards (48×2GB)
- ✧ 12.8GB/s memory bandwidth

Expansion

- ◇ Three PCI-X 64-bit/133MHz slots
- ◇ Six PCI-X 64-bit/66MHz slots
- ◇ Two PCI slots preloaded with core I/O cards
- ◇ One PCI 64/33MHz slot for graphics/USB card (optional)

Drives

- ◇ Four internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug, each pair of drives is connected to one separate controller and each drive in each pair is on a separate channel
- ◇ One open bay for removable SCSI media drives — DVD/DDS

4.43.3 External connectors

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network with web console (on management processor card)
- ◇ Ultra160 SCSI 68-pin
- ◇ Three DB9 male RS232C serial (console, remote console, general purpose)
- ◇ Four USB 2.0 ports (optional)
- ◇ VGA graphics (optional)

4.43.4 References

Articles

- ◇ Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper²¹⁶ (PDF)
Hewlett-Packard Development Company (October 2003, first edition, 5982-1595EN)

4.43.5 Operating systems

- ◇ HP-UX 11i v1.6, v2 and v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

²¹⁶http://www.hpsystem.com/pdf/10420_rx2600_rx4640_rx5670_wp_102303.pdf

4.43.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 rate, int	SPEC2000 rate, fp
rx5670 900MHz 1.5MB	673	1151	7.81 2-CPU: 15.5 4-CPU: 30.4	13.3 2-CPU: 24.5 4-CPU: 38.7
rx5670 1.0GHz 3.0MB	807	1431	9.36 2-CPU: 18.6 4-CPU: 36.8	16.6 2-CPU: 30.7 4-CPU: 49.3
rx5670 1.3GHz 3.0MB	1066	1814	12.4 2-CPU: 24.5 4-CPU: 48.6	21.0 2-CPU: 37.3 4-CPU: 57.2
rx5670 1.5GHz 6.0MB	1312	2108	15.2 2-CPU: 30.3 4-CPU: 60.0	24.5 2-CPU: 42.6 4-CPU: 66.4

4.43.7 Physical dimensions/Power

- ◇ 7U (rack-mount) height, 482×7740 mm width/depth
- ◇ 72.6 kg maximum weight
- ◇ 930W hot-swap power supplies (two standard, optional third)

4.44 HP zx2000

4.44.1 Overview

The HP zx2000 workstation are the Itanium/IA64 brothers of the PA-8800/PA-8900 C8000 workstations. Build around the same HP zx1 chipset, the zx2000 is very similar to the C8000 but delivered with Itanium 2 processors. The system is built in a sleek and quiet tower casing and also available with a rack-mount option. Relative shortly after the zx2000 HP dropped Itanium *workstations* from its portfolio. The remaining HP-UX/Itanium offerings are IA64 server systems (the *Integrity rx*).

Time of introduction: 2002, discontinued: September 2004, with prices at time of introduction between US \$4,000 (entry configuration), \$6,000 (average) and \$11,000 (large).

4.44.2 Internals

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1	Itanium 2 <i>McKinley</i>	900MHz	16/16KB	256KB	1.5MB
1	Itanium 2 <i>Madison</i>	1.4GHz	16/16KB	256KB	1.5MB
1	Itanium 2 <i>Madison</i>	1.4GHz	16/16KB	256KB	4.0MB
1	Itanium 2 <i>Madison</i>	1.5GHz	16/16KB	256KB	1.5MB
1	Itanium 2 <i>Deerfield</i> low-voltage	1.0GHz	16/16KB	256KB	1.5MB

There could be more processor options.
All caches are on-die (L1, L2 and L3).

Chipset

- ✧ HP zx1 chipset (same as in some PA-8800/PA-8900 workstations)
 - zx1 MIO (memory and I/O controller) connects to the processor bus (6.4GB/s), memory bus (4.25GB/s) and six I/O channels (aggregate 3.0GB/s) and contains both memory and cache controllers
 - Four zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.0GB/s on six 0.5GB/s channels
 1. AGP 4x graphics bus on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0GB/s
 3. Four PCI-X 64/66 I/O slots on one channel — 0.5GB/s
 4. Gigabit Ethernet, IDE, USB and audio controllers on PCI 32/33 on one channel — 0.5GB/s
- ✧ Gigabit Ethernet (Intel 82540)
- ✧ Two-channel Ultra160 SCSI controller (optional)
- ✧ Ultra ATA-100 IDE controller (PCI649)
- ✧ PDH controller
- ✧ Serial controller, DUART (16550A-compatible)

- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard management controller (BMC — IPMI interface)

Buses

- ◇ Itanium 2/zx1 processor bus 6.4GB/s
- ◇ zx1 memory bus, 200MHz, 4.25GB/s
- ◇ Six zx1 I/O channels/buses, aggregate 3.0GB/s I/O bandwidth
- ◇ AGP 4x graphics bus on two I/O channels, 1.0GB/s aggregate
- ◇ PCI-X 64/133 I/O bus on two I/O channels, 1.0GB/s aggregate
- ◇ PCI-X 64/66 I/O bus on one I/O channel, 0.5GB/s aggregate
- ◇ PCI 32/33 I/O bus for onboard devices on one I/O channel, 0.5GB/s aggregate
- ◇ SCSI-3 Ultra160 (LVD) storage I/O bus (if optional SCSI controller is installed)
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Takes up to 2GB modules
- ◇ Four slots
- ◇ 512MB minimum (2×256MB)
- ◇ 8GB maximum (4×2GB)
- ◇ 4.25GB/s memory bandwidth

Expansion

- ◇ One PCI-X 64-bit/133MHz slot, full-length
- ◇ Three PCI-X 64-bit/66MHz slots, full-length
- ◇ One PCI-X 64-bit/66MHz slot, half-length
- ◇ All PCI slots are 3.3V
- ◇ One AGP Pro 4x 32-bit slot, 1.5V

Drives

- ◇ Up to two internal 3.5" bays for either Ultra ATA-100 IDE or Ultra160 SCSI hard drives
- ◇ Two half-height 5.25" bays for externally accessible Ultra ATA-100 IDE or SCSI (LVD or SE) drives (DVD/CD)

4.44.3 External connectors

- ◇ TP/RJ45 Gigabit Ethernet
- ◇ Four USB 2.0 ports (two in front, two in rear)
- ◇ Two DB9 male RS232C serial
- ◇ Four phone jacks (microphone, line-in and line-out) on 16-bit audio card
- ◇ Optional IEEE-1394 Firewire ports

4.44.4 References

Manuals

- ◇ **HP Workstation zx2000 - Technical Reference Guide²¹⁷** (PDF) Hewlett-Packard Development Company (April 2003, first edition)

4.44.5 Operating systems

- ◇ HP-UX 11i v1.6 and v2 (v2 May 2005 is the last officially supported version — however it could be later v2 version still work without official support)
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ OpenVMS (however officially unsupported on this platform)
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ Windows Server 2008 Itanium-based Editions
- ◇ Windows Server 2003 Itanium-based Editions

4.44.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
zx2000900MHz	668	1086		12.6

4.44.7 Physical dimensions/Power

- ◇ Tower: 502×268×512 mm height/width/depth
- ◇ Tower: 22kg net weight, 25kg fully loaded
- ◇ Rack-mounted: 4U height, 482×510 mm width/depth
- ◇ Rack-mounted: 17.7kg net weight, 20.6kg fully loaded
- ◇ 643W max. power input (410W typical “workstation configuration”)

²¹⁷<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpv00324/lpv00324.pdf>

4.45 HP zx6000

4.45.1 Overview

The Itanium zx6000s are the dual-processor brothers of the zx2000 workstations. The chassis was designed for rack-mounting (2U) with appropriate rails; with a tower kit it can be converted to a standalone unit. The internal architecture is based on HP's zx1 Itanium chipset, also used in the zx2000 and various PA-RISC servers. In contrast to the zx2000, the zx6000 has slightly higher I/O and double the memory bandwidth and supports three times the amount of memory.

The zx6000 with fast CPUs is probably the fastest HP-UX *workstation*.

Time of introduction: 2002, discontinued: September 2004, with prices at time of introduction between \$7,000 (entry configuration), \$13,000 (average) and \$27,000 (large).

4.45.2 Internals

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 <i>McKinley</i>	900MHz	16/16KB	256KB	1.5MB
1-2	Itanium 2 <i>McKinley</i>	1.0GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Madison</i>	1.3GHz	16/16KB	256KB	3.0MB
1-2	Itanium 2 <i>Madison</i>	1.5GHz	16/16KB	256KB	6.0MB

All caches are on-die (L1, L2 and L3).

Chipset

◇ HP zx1 chipset

- **zx1 MIO** (memory and I/O controller) connects to the processor bus (6.4GB/s), two memory buses (each 4.25GB/s) and seven I/O channels (aggregate 3.5GB/s) and contains both memory and cache controllers
- Six **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.5GB/s on seven 0.5GB/s channels
 1. AGP 4x graphics bus on two channels — 1.0GB/s
 2. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 3. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 4. PCI-X 64/133 I/O slot on one channel — 0.5GB/s
 5. Gigabit Ethernet and Ultra320 SCSI on PCI 64/66 on one channel — 0.5GB/s
 6. IDE, USB, management LAN on PCI 32/33 on one channel — 0.5GB/s

◇ Gigabit Ethernet (Broadcom 5701)

◇ Two-channel Ultra320 SCSI controller (LSI 1030)

◇ Ultra ATA-100 IDE controller (PCI649)

- ◇ PDH controller
- ◇ Serial controller, DUART (16550A-compatible)
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard management controller (BMC — IPMI interface)
- ◇ 10/100 Ethernet for management (Intel 82550)

Buses

- ◇ Itanium 2/zx1 processor bus 6.4GB/s
- ◇ Two independent zx1 memory buses, 266MHz, each 4.25GB/s — aggregate 8.5GB/s memory bandwidth
- ◇ Seven zx1 I/O channels/buses, aggregate 3.5GB/s
- ◇ Three PCI-X 64/133 I/O buses
- ◇ PCI-X 64/66 I/O bus (for SCSI/Gigabit Ethernet onboard)
- ◇ PCI 32/33 I/O bus (for IDE/USB/management onboard devices)
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ AGP 4x graphics bus
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Takes up to 2GB modules
- ◇ Twelve slots
- ◇ 512MB minimum (2×256MB)
- ◇ 24GB maximum (12×2GB)
- ◇ 8.5GB/s memory bandwidth

Expansion

- ◇ Three PCI-X 64-bit/133MHz slots, full-length
- ◇ All PCI slots are 3.3V
- ◇ One AGP Pro 4x 32-bit slot, 1.5V

Drives

- ◇ Three internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug
- ◇ Slimline bay for optional IDE CD or DVD drive

Drive 1 and 2 are on one SCSI channel, drive 3 and the external connector are on the second SCSI channel.

4.45.3 External connectors

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 BT management network
- ◇ Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Four USB 2.0 ports
- ◇ Two DB9 male RS232C serial

4.45.4 References

Manuals

- ◇ **Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000**²¹⁸ (PDF) Hewlett-Packard Development Company (September 2003, second edition)

4.45.5 Operating systems

- ◇ HP-UX 11i v1.6 and v2 (v2 May 2005 is the last officially supported version — however it could be later v2 version still work without official support)
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ Windows Server 2008 Itanium-based Editions
- ◇ Windows Server 2003 Itanium-based Editions
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ OpenVMS (however officially unsupported on this platform)

4.45.6 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000rate, int	SPEC2000rate, fp
zx6000900MHz	669	1139	7.8 2-CPU: 15.4	13.2 2-CPU: 23.9
zx6000 1.0GHz	807	1422		16.5 2-CPU: 30
zx6000 1.5GHz	1315	2106	15.2 2-CPU: 30.4	24.4 2-CPU: 42.4

²¹⁸<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpno4096/lpno4096.pdf>

4.45.7 Physical dimensions

- ◇ Tower: 494×295×675 mm height/width/depth
- ◇ Tower: 22kg net weight, 25kg fully loaded
- ◇ Rack-mounted: 2U height, 483×679 mm width/depth
- ◇ Rack-mounted: 17kg net weight, 22kg fully loaded

4.46 RDI PrecisionBook

4.46.1 Overview

The PrecisionBook portable workstations from **RDI (Tadpole)**²¹⁹ are essentially C132L/C160Ls in a laptop case. The PrecisionBooks mostly use the same technology as the HP 9000 workstations with only slight differences. A major addition to the desktop cousins is the integrated Cardbus controller for which Tadpole supplied a driver kit for use in HP-UX. Support for actual Cardbus and PCMCIA devices in these slots was very sparse however (NE2000-based Ethernet as an example). OpenBSD fully supports the Cardbus controller and a range of different Cardbus and PCMCIA devices (Fast-Ethernet, WLAN etc.).

The PrecisionBook laptop case was used for other RDI RISC laptops as well, for example their Ultra-SPARC systems.

Introduced in 1998 for a list price of \$14,995 (180MHz version).

4.46.2 Internals

CPU

- ◇ PrecisionBook 132: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- ◇ PrecisionBook 160: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- ◇ PrecisionBook 180: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache

The external L2 cache is optional but was supplied with most systems.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Dino GSC-to-PCI bridge
- ◇ Phantom PseudoBC GSC+ port
- ◇ Visualize-EG (*Graffiti*) graphics
- ◇ 1MB flash memory
- ◇ Intel 82503 Ethernet transceiver, media auto-selection

²¹⁹<http://www.tadpolecomputer.com/>

- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ Two Cirrus CL-PD6832 PCI-CardBus bridges
- ◇ CMD PCI0643 IDE/UDMA33 controller

Display

- ◇ Either 12.1" (0.24mm dot pitch) or 14.1" (0.28mm dot pitch) active matrix LCD — 14-inch PrecisionBooks were the most frequent
- ◇ XGA resolution (1024×768)
- ◇ 16M colors
- ◇ 60Hz refresh
- ◇ External monitor output supports VGA, SVGA, XGA, SXGA and 1600×1200 resolutions at refresh rates of 60, 72 and 75Hz
- ◇ At XGA resolution the LCD and an external monitor can be used simultaneously; with different resolutions on the external monitor the LCD blanks

Human Input

- ◇ PS/2-compatible, 97-key keyboard
- ◇ Three-button trackpad

Energy

- ◇ Lithium-Ion battery with 40Wh capacity, 450g
- ◇ About 0.5-1 hours of battery capacity
- ◇ Recharge time of 2.5 hours when powered off
- ◇ Laptop draws about 70W continuous
- ◇ AC adapter provides 19V (DC) 3.68A, non-standard pinout (though there are some with a standard plug)

Buses

- ◇ GSC-2 general system-level I/O bus
- ◇ PCI-32/33 device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus disk I/O
- ◇ PDH bus, peripheral interface connecting to flash memory, NVRAM and PSM bus
- ◇ PSM bus, provides connection to the power-supply module

Memory

- ◇ Proprietary ECC modules, 60ns, 144-bit wide bus
- ◇ Two sockets
- ◇ 32-256MB modules (with 16Mbit or 64Mbit DRAMs in either 1M×16 or 4M×16 configuration)
- ◇ 32MB (1×32) minimum, 512MB (2×256) maximum

Expansion

- ◇ Two Cardbus slots, for Cardbus and PCMCIA expansion cards

Drives

- ◇ Two trays for 2.5" IDE hard drives with SCSI converter or for very rare 2.5" SCSI drives
- ◇ Since 2.5-inch SCSI drives were so rare RDI supplied regular IDE notebook drives together with a special IDE-SCSI converter from ADTXw—in the References section is a link to further details

4.46.3 External connectors

- ◇ 50-pin HD SCSI-2 single-ended
- ◇ TP/RJ45 10Mbit Ethernet
- ◇ VGA 15-pin Dsub graphics connector
- ◇ Two PS/2 connectors for keyboard/mouse
- ◇ Four phone jacks (microphone, headphones, line-in and ?)
- ◇ 15-pin connector for external floppy
- ◇ High-pin-count connector for docking station
- ◇ Connector for special I/O breakout cable for:
 - Two DB9 male RS232C serial
 - DB25 female parallel
 - AUI 10Mbit Ethernet

4.46.4 References

Manuals

- ◇ PrecisionBook hardware reference guide²²⁰ (PDF, 2.0MB)
- ◇ PrecisionBook user guide²²¹ (PDF, 1.4MB)

²²⁰<http://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-refguide.pdf>

²²¹<http://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-userguide.pdf>

Other

- ◇ RDI software for HP-UX 10.20 installation guide²²² (PDF, 0.8MB)
- ◇ RDI software release notes²²³ (PDF, 0.1MB)
- ◇ ADTX SCSI-IDE converters²²⁴ information from Michael Shalayeff.

4.46.5 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs very nicely.
 - 11.00 and 11i: run nicely
- ◇ Linux: should work.
- ◇ NetBSD: should work.
- ◇ OpenBSD: works fine.

4.46.6 Benchmarks

Model	SPEC95, int	SPEC95, fp
PrecisionBook 132	6.49	6.54
PrecisionBook 160	7.78	7.39
PrecisionBook 180	9.22	9.43

²²²<http://ftp.tadpole.com/support/Precisionbook/Manuals/hpux-10-2-installation-guide.pdf>

²²³<http://ftp.tadpole.com/support/Precisionbook/Manuals/rdi-software-release-notes.pdf>

²²⁴<http://mickey.lucifier.net/adtx/>

4.47 SAIC Galaxy 1100

4.47.1 Overview

The SAIC²²⁵ Galaxy 1100 is a portable PA-RISC workstation based on the regular HP 9000/712 workstation in a ruggedized, portable case. However it is not a notebook since it lacks a battery and needs to be connected to standard AC power input.

The Galaxy 1100 is a very rare system, originally built for military/intelligence applications to the following standards:

- ◇ Portable requirements: *Navy TAC-4*
- ◇ Shock: *Federal Test Method Standard 101C, Method 5007.1 free-fall drop test*
- ◇ Airborne: *MIL-STD-740-1, Grade C, Table 1*

SAIC developed several special I/O devices attached to the mainboard via GIO/TSIO expansion cards.

4.47.2 Internals

CPU

- ◇ PA-7100LC 60MHz with 1KB on-chip L1 and 64KB off-chip L1 cache
- ◇ PA-7100LC 80MHz with 1KB on-chip L1 and 256KB off-chip L1 cache

The 1KB on-chip L1 cache is not really a true cache.

Chipset

- ◇ LASI ASIC, which features:
 - NCR 53C710 8-bit single-ended SCSI-2
 - Intel 82596CA 10Mb Ethernet controller
 - WD 16C522 compatible parallel
 - Harmony CD/DAT quality 16-bit stereo audio
 - NS 16550A compatible serial
- ◇ Artist graphics, 8-bit
- ◇ Intel 82503 Ethernet transceiver, media auto-selection
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ WD37C65C Floppy controller
- ◇ Two AM29F010 Flash EPROMs
- ◇ PCMCIA controller

²²⁵<http://www.saic.com>

Display

- ◇ 10.4" active matrix LCD
- ◇ XGA resolution, *i.e.*, 1024×768
- ◇ 256 colors (8-bit color depth)
- ◇ 60Hz refresh

Human Input

- ◇ PS/2-compatible, 84-key integrated QWERTY keyboard with 12 function keys
- ◇ Trackball and three-button pad

Buses

- ◇ GSC system level I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 72-pin ECC SIMMs, same as on standard HP 9000 712
- ◇ (Original documentation describes proprietary memory modules)
- ◇ 8-32MB modules
- ◇ Four sockets
- ◇ 16MB (2×8) minimum, 128MB (4×32) maximum
- ◇ Memory has to be installed in pairs, starting from slot 0, which is the closest slot to the drives.

Expansion

- ◇ Two PCMCIA slots, for either two Type I/II or one Type III PCMCIA card

Drives

- ◇ One 3.5" Fast-Narrow 50-pin SCSI-2 hard drive
- ◇ One 3.5" 1.44MB Floppy drive

4.47.3 External connectors

- ◇ 50-pin HD SCSI-2 Fast-Narrow single-ended
- ◇ DB9 male RS232C serial (up to 115200 baud)
- ◇ DB25 female parallel

- ◇ TP/RJ45 10Mbit Ethernet
- ◇ 15-pin AUI 10Mbit Ethernet
- ◇ HD15 VGA
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Three phone jacks (microphone, headphones and line-in)

4.47.4 Operating systems

- ◇ HP-UX: every 32-bit release from 10.20-11.11 works.
 - 10.20: runs nice.
 - 11.00 and 11i: run ok.
- ◇ Linux: should work.
- ◇ NetBSD: should work.
- ◇ OpenBSD: works fine, although some I/O devices are not supported at the moment (*e.g.*, the PCMCIA controller).

4.47.5 References

Website

- ◇ **SAIC Galaxy 1100 product page**²²⁶ (archive.org mirror) Old product page with photos and details on the SAIC. Science Applications International Corporation (1996). Archive.org mirror accessed 2 Oct 2007.

4.47.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
Galaxy 1100 80MHz	99	122	3.12	3.55

4.47.7 Physical dimensions

- ◇ 114×412×311 mm height/width/depth
- ◇ 8.2kg net weight

²²⁶<http://web.archive.org/web/19961115101405/http://www.saic.com/it/stp/galaxy/index.html>

4.48 Convex Exemplar SPP1000, SPP1200 & SPP1600

4.48.1 Overview

The Convex Exemplar SPP1x00 are scalable 32-bit mainframe/technical computing systems, with either PA-7100 (SPP1000) or PA-7200 (SPP1200 and SPP1600) processors. Previous Convex designs used custom Convex processors, with the SPP line Convex switched to third-party processors with the HP PA-RISC. This probably colluded with the close collaboration between Convex and HP starting in the early 1990s, which resulted in the joint HP/Convex marketed Exemplar SPP2000 (the direct 64-bit successor of the SPP1x00s with a slightly modified architecture) and the takeover of Convex by HP in 1994, which resulted in the HP-branded V-Class servers (the 64-bit non-clusterable HP 9000/V2200 and V2250 and the up to four-way clusterable HP 9000/V2500 and V2600).

The 32-bit Convex SPP1x00 systems consist of three distinct system building concepts, the CD compact systems, the XA eXtended Architecture hypernodes and the XA clusters:

- ◇ SPP1000/CD, SPP1200/CD, SPP1600/CD: single “compact” systems — the documentation is not really clear, this could either be special systems with up to sixteen processors, or — more likely —, two SPP XA Hypernodes coupled together and sold as a single, non-clusterable system.
- ◇ SPP1000/XA, SPP1200/XA, SPP1600/XA Hypernode: a single Hypernode/*eXtended Architecture* (XA) SPP system with up to eight processors and provisions for linking up via SCI to other systems.
- ◇ SPP1000/XA, SPP1200/XA, SPP1600/XA Cluster: a multiple Hypernode *eXtended Architecture* (XA) SPP system, with up to sixteen SPP1x00/XA Hypernodes coupled via SCI/TCI interconnection rings; these XA clusters can have up to 128 processors in their maximum configuration. The resulting interconnected Exemplars are then *ccNUMA* computers, a *cache-coherent Non-Uniform Memory Access* (for a detailed explanation cf. for example the **ccNUMA section on the Wikipedia Non-Uniform Memory Access page**²²⁷).

The internal Exemplar architecture is based on a 5x5 crossbar with the central internal “switching” component (the crossbar) connecting the resources to each other by forming matrix connections between the devices’ input and output ports (“5x5” because the crossbar has five ports for processors, memory and I/O).

The Nodes and Clusters are controlled and booted via a separate workstation connected to it, frequently a IBM RS/6000 computer running AIX, which faced the Exemplar’s console and control I/O (in the case of a cluster only one node had a control workstation). Also apparently used were HP 9000/715 workstations running as “teststation.”

Introduced: 1994 (SPP1000), 1995 (SPP1200), 1996 (SPP1600) for \$145,000-\$750,000 (SPP1000/CD), \$550,000 to \$8 million (SPP1000/CD), \$160,000 (two-CPU SPP1200/CD) and \$586,000 (eight-CPU SPP1200/XA).

4.48.2 Internals

CPU

- ◇ SPP1000/CD: 2-16 PA-7100 100MHz with 1/1MB off-chip I/D L1 cache each
- ◇ SPP1000/XA Hypernode: 2-8 PA-7100 100MHz with 1/1MB off-chip I/D L1 cache each

²²⁷http://en.wikipedia.org/wiki/Non-Uniform_Memory_Access#Cache_coherent_NUMA_.28ccNUMA.29

- ◇ SPP1000/XA Cluster: 8-128 PA-7100 100MHz with 1/1MB off-chip I/D L1 cache each
- ◇ SPP1200/CD: 2-16 PA-7200 120MHz with 256/256KB off-chip I/D L1 cache each
- ◇ SPP1200/XA Hypernode: 2-8 PA-7200 120MHz with 256/256KB off-chip I/D L1 cache each
- ◇ SPP1200/XA Cluster: 8-128 PA-7200 120MHz with 256/256KB off-chip I/D L1 cache each
- ◇ SPP1600/CD: 2-16 PA-7200 120MHz with 1/1MB off-chip I/D L1 cache each
- ◇ SPP1600/XA HyperNode: 2-16 PA-7200 120MHz with 1/1MB off-chip I/D L1 cache each
- ◇ SPP1600/XA Cluster: 8-128 PA-7200 120MHz with 1/1MB off-chip I/D L1 cache each

It is not quite clear how the CD models relate to the XA models—the XA clusters consist of several 2-8 processor hypernodes while the CD models were shipped with up to 16 processors. Either the CDs are different machines than the XA hypernodes or they are simply two XA hypernodes coupled together, without any additional SCI/CTI expansion possibilities.

Chipset

The chipset is based completely on an own Convex design and centers around the Convex five-port crossbar, later improved on the SPP2000 with eight ports and used in HP's V-Class.

1. **5x5 nonblocking crossbar**, with five crossbar ports, is the central part of the system, it connects to four “functional units” (memory, SCI links and processor) and with the fifth port to the local system I/O. The four functional units contain each a memory controller, SCI controller and an “agent” for two processors. Memory and processor use different data links to the crossbar—memory access *always* goes over the crossbar, even from a processor to the memory in the same functional unit. Each crossbar port has a data rate of 250MB/s, giving the crossbar a combined peak bandwidth of 1.25GB/s. The crossbar is implemented in Gallium arsenide gate arrays (GaAs, 250K transistors), quite a rarity, since it was very expensive and difficult to handle.
2. **Four CPU Agents** attach to the crossbar and provide access for the processors to the memory via the crossbar over a 250MB/s crossbar port shared with the memory controller (see below).
3. **Four Convex Coherent Memory Controllers (CCMCs)** attach each one four-way interleaved memory board to the crossbar. The CCMCs additionally do cache coherency and interface to the Convex's SCI (CTI) link for inter-hypernode connection. [It is not quite clear if the CCMCs share the whole 250MB/s port/data connections with the CPU agents on the same functional unit, or if CCMC and CPU agent attach to separate lines of the crossbar port—*Ed.*] The CTI interface—or the complete CCMC—were apparently also GaA chips.
4. **Exemplar I/O (Input/Output) Subsystem** connects to the fifth 250MB/s crossbar port and attaches the I/O subsystem controllers to the crossbar and this memory and processors.

Buses

- ◇ Total crossbar bandwidth 1.25GB/s (five 250MB/s ports)
- ◇ CPU/Memory bandwidth 1.0GB/s (four 250MB/s ports shared with memory)
- ◇ I/O bandwidth 250MB/s (one crossbar port)
- ◇ SPP1000: Four SBus I/O buses for expansion slots

- ◇ SPP1200/SPP1600: Eight SBus I/O buses for expansion slots
- ◇ Attachments to SCI rings, interconnection via four one-dimensional rings bandwidth of 2.4GB/s (each ring has a data rate of 600MB/s, with a clock of 150MHz [both edges] and a width of 16 bit)
- ◇ SCSI-2 storage I/O bus

Memory

- ◇ DRAM
- ◇ Two to eight memory boards per node
- ◇ Memory is up to eight-way interleaved per node
- ◇ XA single nodes: up to 2GB of memory (512MB per memory board)
- ◇ CD nodes: up to 4GB of memory

Expansion

- ◇ XA single nodes: 8 SBus slots
- ◇ CD nodes: 16 SBus slots
- ◇ (This is apparently really the same **SBus**²²⁸ as the one used by Sun in their earlier workstations —IEEE 1496)

Drives

- ◇ 20 internal SCSI drives

4.48.3 Clustering

Multiple SPP1000/XA systems can be connected together to form a single large system.

- ◇ Up to sixteen SPP1000/SPP1200/SPP1600 (XA models) can be clustered together to form a system with up to
 - 128 processors
 - 32GB of RAM
 - 64 SBus slots
 - 320 SCSI drives
- ◇ Clustered SPP Exemplar are ccNUMA computers.
- ◇ Multiple systems (nodes) are connected via four CTI rings: each uni-directional ring attaches to the same CCMC memory controller on different nodes (all nodes attach with their first CCMC to the first ring, with their second CCMC to the second ring, and so on).

²²⁸<http://en.wikipedia.org/wiki/SBus>

- ◇ The four rings are implementations of the IEEE Standard 1596-1992 (SCI), called by Convex CTI — Convex Toroidal Interconnect.
- ◇ Each ring is only unidirectional and has a bandwidth of 600MB/s (16-bit differential, 300MHz clock)
- ◇ Complete CTI bandwidth is thus 2.4GB/s.
- ◇ Each node's main memory is globally accessible from other nodes on the CTI network (that is, local memory is globally shared).
- ◇ Memory access to global memory goes from the processor through the local crossbar to the local functional unit whose memory controller is associated with the remote memory — it attaches to the same CTI ring the remote memory/CCMC attaches to. (The *A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar* paper in the References has a detailed discussion of the CTI ring topology, memory access and performance.)

4.48.4 External connectors

- ◇ SCSI depending on installed controller
- ◇ Console/control connections for the control workstation (teststation)

4.48.5 References

Manuals

- ◇ *SPP₁₂₀₀/CD Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation)
- ◇ *SPP₁₂₀₀/XA Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation) [did not find appropriate URLs for these two Convex data sheets — *Ed.*]

Articles

- ◇ **A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar**²²⁹ (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a **mirrored PDF version from citeseer**²³⁰ (accessed August 2008)])
- ◇ **Characterizing Shared Memory and Communication Performance: A Case Study of the Convex SPP-1000**²³¹ (Postscript) Gheith A. Abandah and Edward S. Davidson (January 1996: University of Michigan. Accessed August 2008)
- ◇ **An Empirical Evaluation of the Convex SPP-1000 Hierarchical Shared Memory System**²³² (PDF) Thomas Sterling, et al. (1995: Proceedings of the IFIP WG10.3 working conference on Parallel architectures and compilation techniques. Citeseer mirror accessed April 2009)

²²⁹<http://www.cse.ohio-state.edu/hpcs/WWW/HTML/publications/papers/TR-97-6.ps.Z>

²³⁰<http://citeseer.ist.psu.edu/cache/papers/cs/6798/http:zSzzSzwww.cs.wm.edu:zShpcszSzWWWzSzHTMLzSzpublicationszSz.zSzpaperszSzTR-97-6.pdf/castaneda97comparative.pdf>

²³¹<http://www.eecs.umich.edu/PPP/CSE-TR-277-96.ps>

²³²<http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.53.8760&rep=rep1&type=pdf>

Other

- ◇ **Exemplar 1200 Architecture**²³³ presentation (FTP, Postscript) Beth Richardson? (N.d.: NCSA. Google archive accessed August 2008)

4.48.6 Operating systems

- ◇ Convex SPP-UX, a heavily modified Mach-based operating system, which *looks* familiar to HP-UX but is a completely different design. The later HP V-Class are able to run stock HP-UX (which was modified specially for the V-Class architecture).

4.48.7 Benchmarks

Model	SPEC92 fp	SPEC95 int	SPEC95 fp	SPEC95 rate, int	SPEC95 rate, fp
SPP1000		3.27	3.98		
SPP1200	185				
SPP1600				8-CPU: 290 16-CPU: 541 32-CPU: 996	8-CPU: 383 16-CPU: 744 32-CPU: 1444

4.48.8 Physical dimensions

- ◇ SPP1200/XA: 71×112×178 cm
- ◇ SPP1200/XA: 404 kg maximum weight
- ◇ SPP1200/CD: “smaller” tower-like systems (thus “compact”)
- ◇ SPP1200/CD: 159 kg maximum weight
- ◇ SPP1200/CD: 46×99×89 cm
- ◇ The cabinets are air-cooled
- ◇ XA systems: up to two cabinets can be mechanically stacked

²³³<http://ftp.ncsa.uiuc.edu/ncsapubs/HPCTraining/SPP1200.ps>

4.49 HP/Convex SPP2000 (S-Class/X-Class)

4.49.1 Overview

The HP/Convex Exemplar SPP2000 are large scalable PA-RISC computing servers and the direct predecessors of the later HP V-Class (V2200, V2500 et al). Originally developed by Convex, the SPP2000 are based on a crossbar architecture with the central internal “switching” component connecting the resources to each other by forming matrix connections between the devices’ input and output ports.

A single SPP2000 computer can hold up to sixteen 64-bit PA-8000 processors with 16GB of memory in a single *Node*—the resulting system is called *S-Class* (according the HP’s nomenclatura). The SPP2000 can form a large-scale system by connecting single Nodes with SCI links (forming rings) into a larger cluster (*Wall*) of up to 32 nodes/512 processors. The resulting interconnected systems are called *X-Class*, in effect consisting of several S-Classes. Interconnected X-Classes are *ccNUMA* computers, *cache-coherent Non-Uniform Memory Access* (for a detailed explanation cf. for example the *ccNUMA* section on the *Wikipedia Non-Uniform Memory Access* page²³⁴). Interestingly, the clustering capabilities of the SPP2000’s successors, the V2500, have been reduced significantly—in contrast to the 32-node maximum of SPP2000 clusters, V2500s only can be clustered to groups of four.

As the other Exemplar systems, the SPP2000/S-Class are operated and controlled via so-called “teststations,” Unix workstations that connect to a central management board in the single nodes which provides booting, system monitoring and diagnostics, and console connections. (These teststations were either IBM RS/6000 AIX systems or later, more common, HP 9000 workstation running HP-UX.)

Introduced: 1996-97 with prices at time of introduction of \$189,000 (SPP2000 Node/HP S-Class, four-CPU) to \$720,000 to \$3 million (SPP2000 Cluster, HP X-Class).

4.49.2 Internals

CPU

- ◇ SPP2000 Node/S-Class: 4-16 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache each
- ◇ SPP2000 Cluster/Wall/X-Class: 32-512 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache each

Chipset

The SPP2000 is based on the Exemplar crossbar architecture which connects the CPU and I/O to the system main memory.

1. **8x8 nonblocking crossbar** is the central part of the system, it connects the memory to the processor buses and I/O channels. There are eight ports for “agents” for CPUs and I/O—each agent connects to two CPUs and one I/O channel—, and eight ports for memory. Each crossbar port has a path width of 64-bit, giving it 960MB/s peak bandwidth. The peak raw bandwidth of the crossbar is 15.3GB/s combined. The crossbar in the original Exemplar design (SPP1x00) was built of GaA chips, the SPP2000’s in standard CMOS (1.1M transistors).

²³⁴http://en.wikipedia.org/wiki/Non-Uniform_Memory_Access#Cache_coherent_NUMA_.28ccNUMA.29

2. **Eight Data Mover/Agents** attach to the crossbar and provide access for the processors (Runway buses) and I/O controllers (I/O channels) to the memory via the crossbar over a 1.9GB/s datapath (four 32-bit, unidirectional buses from two ports on the Agent connect to two crossbar ports). The I/O channels on the agent have a maximum bandwidth of 240MB/s. Each Agent has two Runway processors buses (64-bit, bidirectional) which have an aggregate raw bandwidth of 960MB/s.
3. **Eight PCI controller** connect the 240MB/s I/O channels/PCI buses to the Agents.
4. **Eight Memory controllers** attach each one four-way interleaved memory board to the Hyperplane crossbar. Each Memory controller has a bandwidth of 1.9GB/s. The memory controllers probably also interface with the CTI interconnection.

Buses

- ◇ Total crossbar bandwidth 15.3GB/s (intra-crossbar)
- ◇ CPU bandwidth 7.5GB/s (CPU-to-Agent, eight Runway 960MB/s buses)
- ◇ Memory bandwidth 15GB/s (memory-to-crossbar, sixteen 960MB/s links)
- ◇ I/O bandwidth 1.9GB/s (eight 240MB/s channels, I/O channel-to-Agent)
- ◇ Eight PCI-32 I/O buses for expansion slots (each 240MB/s)
- ◇ Attachments to SCI rings/CTI (“Coherent Toroidal Interconnect”) via two rings (X-ring and Y-ring), Node-to-Node bandwidth of 3.84GB/s, the rings operate at a clock of 120MHz with a width of 32 bit
- ◇ SCSI-2 Ultra main storage I/O bus

Memory

- ◇ SDRAM DIMMs
- ◇ Two to eight memory boards per node
- ◇ Memory is up to four-way interleaved per memory board and up to 32-way interleaved per node
- ◇ SPP2000 Node/S-Class: 1GB minimum, 16GB maximum
- ◇ SPP2000 Wall/X-Class: 512GB maximum (with 32 nodes)

Expansion

- ◇ 24 PCI 32-bit slots on eight PCI 32-bit channels

Drives

- ◇ 20 internal Ultra SCSI drives

4.49.3 Clustering

Multiple Exemplar SPP2000/HP S-Class systems can be connected together to form a single large system, a “Wall”/X-Class.

- ◇ Up to two 32 single nodes can be clustered together to form a system with up to
 - 512 processors
 - 512GB of RAM
 - 768 PCI slots
 - 640 SCSI drives
- ◇ Clustered SPP2000s/X-Class are ccNUMA computers; they are not fully conformant to the PA-RISC 2.0 specification (and thus do not run standard HP-UX).
- ◇ Multiple systems are connected via two CTI rings: these links attach to the eight memory controllers of a node. A single system attaches to other single “nodes” and their respective crossbars with a node-to-node data rate of 3.8GB/s.
- ◇ The two rings are called X-ring and Y-ring.
- ◇ The links are implementations of the IEEE SCI from Convex — Convex Toroidal Interconnect.
- ◇ Each node’s main memory is globally accessible from other nodes on the CTI network (that is, local memory is globally shared).
- ◇ A part of each system’s main memory is reserved for cache memory for the CTI network (configured statically at boot time).

4.49.4 External connectors

- ◇ 68-pin VHDCI Ultra LVD external SCSI
- ◇ Three DB9 male RS232C serial (local console, remote console, general purpose) via a DB25 “M cable”
- ◇ 10/100Mbit Ethernet TP/RJ45
- ◇ 10/100Mbit Ethernet TP/RJ45 *LAN console*

4.49.5 ROM update

There is an firmware update available for the SPP2000 which contains the latest version 4.2.1.

- ◇ `PF_CV220421.txt`²³⁵ has details about the contents and installation of the patch.
- ◇ `PF_CV220421.tar.gz`²³⁶ contains the patch.

²³⁵ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CV220421.txt

²³⁶ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CV220421.tar.gz

4.49.6 References

Articles

- ◇ **Exemplar System Architecture**²³⁷ Hewlett-Packard/Convex (Januar 1997, archive.org mirror, access August 2008)
- ◇ **SPP 2000 Architecture**²³⁸ presentation (FTP, Postscript) Beth Richardson (N.d.: NCSA. Google archive accessed August 2008)
- ◇ **A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar**²³⁹ (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a **mirrored PDF version from citeseer**²⁴⁰ (accessed August 2008)]

4.49.7 Operating systems

- ◇ Convex SPP-UX, a heavily modified Mach-based operating system, which *looks* familiar to HP-UX but is a completely different design. The later HP V-Class are able to run stock HP-UX (which was modified specially for the V-Class architecture).

4.49.8 Benchmarks

Model	SPEC95 int	SPEC95 fp	SPEC95 rate, int	SPEC95 rate, fp
SPP2000/S-Class/X-Class	11.8	18.7	92.5 2-CPU: 183 4-CPU: 363 6-CPU: 539 8-CPU: 713 10-CPU: 867 12-CPU: 1012 16-CPU: 1307	141 2-CPU: 276 4-CPU: 524 6-CPU: 739 8-CPU: 935 10-CPU: 1085 12-CPU: 1220 16-CPU: 1413

4.49.9 Physical dimensions

- ◇ Single node: 736×914×889 mm
- ◇ Weight of about 250kg

²³⁷http://web.archive.org/web/19970629221930/www.convex.com/prod_serv/exemplar/sx-class/exemplar2.html#sclass

²³⁸<http://ftp.ncsa.uiuc.edu/ncsapubs/HPCTraining/SPP2000.ps>

²³⁹<http://www.cse.ohio-state.edu/hpcs/WWW/HTML/publications/papers/TR-97-6.ps.Z>

²⁴⁰<http://citeseer.ist.psu.edu/cache/papers/cs/6798/http:zSzzSzwww.cs.wm.edu:zShpcszSzWWWzSzHTMLzSzpublicationszSz.zSzpaperszSzTR-97-6.pdf/castaneda97comparative.pdf>

4.50 HP V2200 & V2250

4.50.1 Overview

The V2250 and V2250 are large-scale scalable PA-RISC servers, with up to sixteen 64-bit PA-RISC processors in a single “cabinet.”

The V-Class servers are based on a crossbar architecture — one central internal “switching” component links the various computing resources to each other by connecting the devices’ inputs to other devices’ output ports (in effect forming matrix connections). The V2200 and V2250 use HP’s own HyperPlane crossbar chipset, consisting of four central crossbar ASICs and various other chipset components to attach memory, processors and I/O.

The architecture is a direct continuation from the Convex *Exemplar* — the 32-bit SPP1X00 and 64-bit SPP2000 S-Class and X-Class, designed by Convex and later bought by HP, use a similar crossbar-based system design. Interestingly, the V2200/V2250 use basically the same design as the SPP2000 S-Class (single node) but without the SCI/TCI links for interconnecting several nodes into a larger system (wall). The V2200/V2250 do not carry the chipset attachments and SCI links for this interconnection (or they were disabled in ROM/hardware) — the V2500/V2600 successors again were delivered with the interconnection technology (crossbar/memory-attachment to the SCI rings) of the SPP2000. One possible cause could be the fact that an cluster of several nodes did not conform fully to the PA-RISC 2.0 specification and several changes were needed for running stock HP-UX both in the firmware (“emulates” a fully compliant PA-RISC system) and HP-UX itself. Either these changes were not ready when the V2200/V2250 shipped or V22xos were simply designated to be single-node systems, with larger requirements needing systems like the existing clusterable HP/Convex SPP2000 X-Class or the later V2500/V2600.

The V2200s and V2250s are controlled via a so-called “teststation,” which runs its own HP-UX operating system and controls and monitors the V-Class server. This teststation is a standard HP 9000/712 workstation (A4082A) with special teststation hardware (second ethernet and serial boards, available separately as B6044A) and software. The teststation connects to the Core Utilities Board (CUB), which provides booting, system monitoring and diagnostics, and console connections (connected via one LAN and one special serial link).

Introduced: November 1997 (V2200), March 1998 (V2250).

4.50.2 Internals

CPU

- ◇ V2200: 4-16 PA-8200 200MHz with 2/2MB off-chip I/D L1 cache each
- ◇ V2250: 4-16 PA-8200 240MHz with 2/2MB off-chip I/D L1 cache each

Chipset

The V-Classes are based on the HP HyperPlane crossbar which connects the CPU and I/O to the system main memory.

1. **HyperPlane crossbar**, 8x8, non-blocking, consists of **four Exemplar Routing Attachment controllers (ERACs)** and is the central part of the system, it connects the memory to the processor

buses and I/O channels. There are eight ports for “agents” for CPUs and I/O — each agent connects to two or four CPUs and one I/O channel —, and eight ports for memory. Each crossbar port has a path width of 64-bit, giving it 960MB/s peak bandwidth. The peak raw bandwidth of the HyperPlane crossbar/ERACs is 15.3GB/s combined.

2. **Eight Exemplar Processor Agent controllers (EPACs)** attach to the crossbar and provide access for each two processors (Runway buses) and one I/O controller to the memory via the crossbar over a 1.9GB/s datapath (four 32-bit, unidirectional buses from two ports on the PAC connect to two Hyperplane crossbar ERACs; each EPAC thus communicates with only two of the system’s four ERACs). The I/O channels on the agents have a maximum bandwidth of either 120 or 240MB/s. Each EPAC has two Runway processors buses (64-bit, bidirectional) which have an aggregate raw bandwidth of 960MB/s for two processors per EPAC.
3. **Eight Exemplar PCI-bus Interface controller (EPICs)** connect the 240MB/s I/O channels/PCI buses to the EPACs.
4. **Eight Exemplar Memory Access controllers (EMACs)** attach each one 32-way interleaved memory board to the Hyperplane crossbar. Each EMAC has a bandwidth of 1.9GB/s (four 32-bit, unidirectional buses from two ports on the EMAC connect to two Hyperplane crossbar ERACs).
5. The **Exemplar Core Utilities board (ECUB)** provides interrupts and the central system logic, it connects to the Exemplar system Routing board (ENRB). The Core Logic Bus from the ECUB attaches to the devices on the EPACs. Included on the ECUB are two custom FPGAs, the Exemplar Processor Utilities controller (EPUC) and the Exemplar Monitoring Utilities controller (EMUC).

The remainder of the system I/O consist of standard HP PCI controllers, frequently shipped in default configuration with one of the following:

- ✧ PCI Fast-wide (FWD) SCSI controller (high-voltage differential/HVD) [A4800A]
- ✧ PCI fibrechannel (FC) controller

Buses

- ✧ Total crossbar bandwidth 15.3GB/s (intra-crossbar)
- ✧ CPU bandwidth 7.5GB/s (CPU-to-EPAC, eight Runway 960MB/s buses)
- ✧ Memory bandwidth 15GB/s (memory-to-crossbar, sixteen 960MB/s links)
- ✧ I/O bandwidth 1.9GB/s (eight 240MB/s channels, I/O channel-to-EPAC)
- ✧ (EPAC bandwidth, EPAC-to-crossbar is also 15GB/s theoretically, with sixteen 960MB/s links for the eight EPACs)
- ✧ Eight PCI-64/33 I/O buses for expansion slots (each 240MB/s)
- ✧ SCSI/storage buses depend on the installed SCSI adapter, likely Fast-wide (HVD)

Memory

- ✧ SDRAM DIMMs
- ✧ Two to eight memory boards
- ✧ Each memory board has 16 slots

- ◇ Memory is up to 32-way interleaved
- ◇ 16GB maximum

Expansion

- ◇ 24 PCI 64-bit 33MHz slots on eight PCI 64-bit channels

Drives

- ◇ 16 internal SCSI drives, exact type depending on installed SCSI adapter, but in any case most like Wide SCSI (Fast)

4.50.3 External connectors

- ◇ External SCSI connection
- ◇ Serial and two Ethernet for the console/Teststation
- ◇ TCI/SCI links for the interconnection to other V-Classes

4.50.4 ROM update

There are several firmware updates available on HP's FTP server for the V-Class systems. The files start with PF_CV2 and can be found in the **firmware catalog**²⁴¹ (text file, FTP) and then **downloaded from ftp.itrc.hp.com**²⁴² (FTP).

4.50.5 References

Manuals

- ◇ **Site Preparation Guide: HP 9000 V-Class Server**²⁴³ Hewlett-Packard Development Company (March 1998, second edition, A3725-96021)

Articles

- ◇ **Architecture HP 9000 V-Class Server**²⁴⁴ (PDF) Hewlett-Packard Company (March 1998, second edition, A3725-96022)

Websites

- ◇ **HP Technical Documentation: Enterprise Servers, Workstations and Systems Hardware: V-Class Server**²⁴⁵ Hewlett-Packard Development Company (2008, accessed August 2008)

²⁴¹http://ftp.itrc.hp.com/firmware_patches/hp/cpu/catalog

²⁴²http://ftp.itrc.hp.com/firmware_patches/hp/cpu/

²⁴³<http://docs.hp.com/en/A3725-96021/index.html>

²⁴⁴<http://docs.hp.com/en/A3725-90004/A3725-90004.pdf>

²⁴⁵<http://docs.hp.com/en/hw.html#V-ClassServer>

4.50.6 Operating systems

- ◇ HP-UX: 11.00 and 11i (v1)

4.50.7 Benchmarks

Model	SPEC95 int	SPEC95 fp	SPEC95 rate, int	SPEC95 rate, fp
V2200	13.8	22.1	1-CPU: 125 4-CPU: 484 8-CPU: 964 12-CPU: 1442 16-CPU: 1865	1-CPU: 4-CPU: 755 8-CPU: 1380 12-CPU: 1909 16-CPU: 2312
V2250	16.4	24.8	16-CPU: 2209	16-CPU: 2471

4.50.8 Physical dimensions

- ◇ 1006×998×859 mm height/width/depth
- ◇ Weight of max about 250kg
- ◇ The cabinets are air-cooled
- ◇ Multiple cabinets can be mechanically stacked

4.51 HP V2500 & V2600

4.51.1 Overview

The V2500 and V2600 are the second generation scalable PA-RISC V-Class servers built upon the Convex Exemplar architecture. They can hold up to 32 64-bit PA-RISC processors in a single “cabinet.” As their Convex SPP2000 predecessors, and contrary to their V2200/V2250 cousins, multiple systems (up to four) can be interconnected via so-called CTI links (independent rings — SCI interconnects). The resulting combined system can have up to 128 CPUs and presents itself to the operating system as a single computer. Architecturally, the interconnected V2500s/V2600s are *ccNUMA* computers, that is *cache-coherent Non-Uniform Memory Access* (for a detailed explanation cf. for example the *ccNUMA* [section on the Wikipedia Non-Uniform Memory Access page](#)²⁴⁶).

The V-Class servers are based on a crossbar architecture — one central internal “switching” component links the various computing resources to each other by connecting the devices’ inputs to other devices’ output ports (in effect forming matrix connections). The V2500 and V2600 use HP’s own HyperPlane crossbar chipset, consisting of four central crossbar ASICs and various other chipset components to attach memory, processors and I/O.

The architecture is a direct continuation from the Convex *Exemplar* — the SPP1X00 and SPP2000 S-Class and X-Class, designed by Convex and later bought by HP, use a similar crossbar-based system design (there based on GaA chips), upgraded in the V-Class more or less only with faster processors and memory. Interestingly, a multi-node V2500/V2600’s system architecture (“SCA”) does not conform fully to the PA-RISC 2.0 reference architecture — the firmware layer emulates a reference-compliant PA-RISC system for the operating system (standard HP-UX 11). However several changes had to be made to the (standard) HP-UX kernel to accomodate the V-Class’s special architecture (also called “technical anomalies” ; cf. the *HP Scalable Computing Architecture* paper in the References).

The V2500s and V2600s are controlled via a so-called “teststation” (also called SSP, Service Support Processor) a separate workstation which runs its own operating system and controls and monitors the V-Class server (this was either a HP 9000/712 or B180L workstation with two Ethernet interfaces running HP-UX 10.20 — earlier Convex systems apparently used IBM RS/6000 workstations running AIX to control the Exemplar systems). The SSP/teststation connects to the Core Utilities Board (CUB), which provides booting, system monitoring and diagnostics, and console connections (connected via one LAN and one special serial link).

Introduced: 1999 (V2500), 2000 (V2600)

4.51.2 Internals

CPU

- ◇ V2500: 2-32 PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- ◇ V2600: 2-32 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache each

Chipset

The V-Class V2500 and V2600 are based on the HP HyperPlane crossbar which connects the CPU and I/O to the system main memory.

²⁴⁶http://en.wikipedia.org/wiki/Non-Uniform_Memory_Access#Cache_coherent_NUMA_.28ccNUMA.29

1. **HyperPlane crossbar**, 8x8, non-blocking, consists of **four Routing Attachment controllers (RACs)** and is the central part of the system, it connects the memory to the processor buses and I/O channels. There are eight ports for “agents” for CPUs and I/O — each agent connects to two or four CPUs and one I/O channel —, and eight ports for memory. Each crossbar port has a path width of 64-bit, giving it 960MB/s peak bandwidth. The peak raw bandwidth of the HyperPlane crossbar/RACs is 15.3GB/s combined.
2. **Eight Processor Agent controllers (PACs)** (also SPAC) attach to the crossbar and provide access for the processors (Runway buses) and I/O controllers (I/O channels) to the memory via the crossbar over a 1.9GB/s datapath (four 32-bit, unidirectional buses from two ports on the PAC connect to two Hyperplane crossbar RACs; each PAC thus communicates with only two of the system’s four RACs). The I/O channels on the agent have a maximum bandwidth of 240MB/s. Each PAC has two Runway processors buses (64-bit, bidirectional) which have an aggregate raw bandwidth of 960MB/s.
3. **Eight PCI-bus Interface controller (SAGA)** connect the 240MB/s I/O channels/PCI buses to the PACs.
4. **Eight Memory Access controllers (MACs)** (also SMAC) attach each one 32-way interleaved memory board to the Hyperplane crossbar. Each MAC has a bandwidth of 1.9GB/s (four 32-bit, unidirectional buses from two ports on the MAC connect to two Hyperplane crossbar RACs)
5. The **Core Utilities board (CUB)** provides interrupts and the central system logic, it connects to the Midplane Interconnect Board (MIB). The Core Logic Bus from the CUB attaches to the devices on the PACs.
6. **Eight Toroidal Access Controller (STACs)** connect to a variation of the Scalable Coherent Interconnect (SCI) to one or two “rings.” The combination of STACs and these (SCI) rings is referred to as Coherent Toroidal Interconnect (CTI).

The remainder of the system I/O consist of standard HP PCI controllers, frequently shipped in default configuration with one of the following:

- ✧ PCI Fast-wide (FWD) SCSI controller (high-voltage differential/HVD) [A4800A]
- ✧ PCI Ultra2-wide SCSI controller (low-voltage differential/LVD) [A5149A]
- ✧ PCI fibrechannel (FC) controller

Buses

- ✧ Total crossbar bandwidth 15.3GB/s (intra-crossbar)
- ✧ CPU bandwidth 7.5GB/s (CPU-to-PAC, eight Runway 960MB/s buses)
- ✧ Memory bandwidth 15GB/s (memory-to-crossbar, sixteen 960MB/s links)
- ✧ I/O bandwidth 1.9GB/s (eight 240MB/s channels, I/O channel-to-PAC)
- ✧ (PAC bandwidth, PAC-to-crossbar is also 15GB/s theoretically, with sixteen 960MB/s links for the eight PACs)
- ✧ Eight PCI-64/33 I/O buses for expansion slots (each 240MB/s)
- ✧ Attachments to CTI/Scalable Computing Architecture (SCA) crossbar interconnection, 3.8GB/s
- ✧ SCSI/storage buses depend on the installed SCSI adapter, most likely either Fast-wide (HVD) or Ultra2-wide (LVD)

Memory

- ◇ SDRAM DIMMs (88-bit or 80-bit)
- ◇ Two to eight memory boards
- ◇ Each memory board has 16 slots: four 4-slot “quadrants”
- ◇ Memory is up to 256-way interleaved
- ◇ 1GB minimum
- ◇ 32GB maximum

Expansion

- ◇ 28 PCI 64-bit 33MHz slots on eight PCI 64-bit channels

Drives

- ◇ 16 internal SCSI drives, exact type depending on installed SCSI adapter, but in any case most like Wide SCSI (Ultra or Fast)

4.51.3 Clustering

Multiple V-Classes can be connected together to form a single large system resulting in a “SCA” (Scalable Computing Architecture) system:

- ◇ Up to four V2500/V2600s can be clustered together to form a system with up to
 - 128 processors
 - 128GB of RAM
 - 112 PCI slots
 - 64 SCSI drives
- ◇ Clustered V-Classes are ccNUMA computers; they are not fully conformant to the PA-RISC 2.0 specification.
- ◇ Multiple systems are connected via two CTI rings: these links attach via the STACs to the eight memory controllers. A single system attaches to one or two other V2500/V2600 “cabinets” and their respective crossbars with a node-to-node data rate of 3.8GB/s.
- ◇ The two rings are called X-ring and Y-ring.
- ◇ The links are implementation of the IEEE *SCI* standard taken over from Convex—Coherent Toroidal Interconnect (earlier: Convex Toroidal Interconnect).
- ◇ Each node’s main memory is globally accessible from other nodes on the CTI network (that is, local memory is globally shared).
- ◇ 32-512MB of each system’s main memory is reserved for cache memory for the CTI network (configured statically at boot time).

4.51.4 External connectors

- ◇ SCSI depends on installed adapter, either Ultra (LVD) or Fast wide (HVD)
- ◇ Serial and Ethernet connections of the teststation/SSP

4.51.5 ROM update

There are several firmware updates available on HP's FTP server for the V-Class systems. The files start with PF_CV2 and can be found in the **firmware catalog**²⁴⁷ (text file, FTP) and then **downloaded from ftp.itrc.hp.com**²⁴⁸ (FTP).

4.51.6 References

Manuals

- ◇ **Operator's Guide HP 9000 V2500 Server**²⁴⁹ (PDF) Hewlett-Packard Company (December 1998, first edition, A5075-96005)

Articles

- ◇ **Architecture Reference Guide V2500 Server**²⁵⁰ (PDF) Hewlett-Packard Company (June 1999, first edition, A5074-90004)
- ◇ **HP Scalable Computing Architecture**²⁵¹ Randy Wright and Arun Kumar (October 2000/revised January 2002: USENIX, Proceedings of the First WIESS Workshop)

Websites

- ◇ **HP Technical Documentation: Enterprise Servers, Workstations and Systems Hardware: V-Class Server**²⁵² Hewlett-Packard Development Company (2008, accessed August 2008)

4.51.7 Operating systems

- ◇ HP-UX: 11.00 and 11i (v1)

4.51.8 Benchmarks

Model	SPEC95 <i>rate, int</i>
V2500	16-CPU: 400232-CPU: 7481
V2600	16-CPU: 516432-CPU: 9315

²⁴⁷http://ftp.itrc.hp.com/firmware_patches/hp/cpu/catalog

²⁴⁸http://ftp.itrc.hp.com/firmware_patches/hp/cpu/

²⁴⁹<http://docs.hp.com/en/A5075-90005/A5075-90005.pdf>

²⁵⁰<http://docs.hp.com/en/A5074-90004/A5074-90004.pdf>

²⁵¹http://www.usenix.org/events/osd100/wiess2000/full_papers/wright/wright_html/index.html

²⁵²<http://docs.hp.com/en/hw.html#V-ClassServer>

4.51.9 Physical dimensions

- ◇ 990×800×940 mm height/width/depth
- ◇ Weight of 223kg
- ◇ The cabinets are air-cooled
- ◇ Multiple cabinets can be mechanically stacked

4.52 Stratus Continuum

4.52.1 Overview

Stratus Technologies²⁵³ built a line of “Ultra High Availability Fault Tolerant” PA-RISC (32-bit PA-7100 and 64-bit PA-8x00) based servers called *Continuum* (with a stated availability of 99.999% and more). These systems feature a great deal of redundancy, peaking in having four CPUs to form one single logical processor. The PA-RISC-powered systems were phased out in 2004 in favor of Intel IA32-based systems (not covered here).

The Stratus Continuum servers ran either Stratus-modified HP-UX 11.00, Stratus VOS (PA-RISC support from release 13.0 until 14.7.2) or FTX, Stratus’ own Unix System V Release 4 multiprocessor OS (however support differed between the 400 and 600/1200 lines).

4.52.2 Hardware Details

I/O

The Continuum 600 and 1200 series are basically the same system, except for the chassis configuration. The 600 has six slots for the main bus (called the **Golf** bus), and the rest of the space is filled with I/O card cages meant for secondary I/O boards. The 1200 has twelve slots for the main bus which occupies the entire width of the chassis. Secondary I/O boards go into a separate chassis. Both models have space for two rows of cooling fans on the top, and two rows of disk drives on the bottom (and also either a QIC or DAT tape drive or CDROM drive). The redundant power supplies with built-in UPS resides at the very bottom.

The main Golf bus is the main interconnect between the “big” boards. It is also redundant and self-checking. The “big” boards consist of the following (all these are FRUs):

- ◇ G7xx - CPU and memory boards (of different number and type of processors, speeds and memory sizes)
- ◇ K450 - 4-channel HVD fast wide SCSI and Ethernet adapter
- ◇ K460 - 4-channel HVD fast wide SCSI and Ethernet adapter
- ◇ K470 - A “carrier board” that can contain up to three PMC (PCI-mezzanine) daughter cards
- ◇ K600 - Adapter to two PK-buses which connects to the secondary I/O card cages

On the 600 chassis, the six slots consists of two for the pair or CPU/memory boards, and four more slots for two pairs of “big” boards. On the 1200 chassis, there are slots for two pairs of CPU/memory boards and four pairs of big boards.

In addition the 600/1200 main chassis also has a pair of Console Controller cards which provides the RS232 console terminal and RSN modem connectivity. This controller also has a command mode that allows the operator to type commands on the console to reset the system, power down, power up, etc. It runs on “housekeeping power” that is independent of the rest of the system. The Console controller also contains some environmental monitoring circuitry that checks the chassis internal temperature and will increase the cooling fan speed if necessary (the fans themselves are also hot-swappable FRUs).

The secondary I/O chassis can be used to plug in a wide array of I/O boards (all Stratus proprietary). These boards are also used on the XA/R line. FTX supported many of the communications boards

²⁵³<http://www.stratus.com>

(ISDN, serial, parallel, X.25, and all sorts of other comm boards). HP-UX did not support many of those, if any. VOS also supported disk and tape I/O through this.

Expansion chassis is available to house additional secondary I/O cards or disk shelves (for large disk farms, etc).

Architecture

Each logical processor is physically two pairs of actual CPUs (that means four physical CPU chips per single logical one).

Each pair is located on a separate FRU. All processors run “lock-stepped” (that is, they do exactly the same thing at the same time). Comparator logic between each two physical CPU pair monitors for discrepancies. If any physical CPU glitches or does something different, the comparator logic will detect the error and take that pair of CPUs offline, while the system continues to run on the other pair. There is no “failover time.” On multi-processor boards, each FRU contains multiple pairs of the logical processor halves.

The memory is self-checking and ECC corrected. If an uncorrectable error occurs, the FRU in which the memory is located will also be taken offline.

The DMA engines for the big I/O boards is designed such that the main memory content is protected from an errant card from scribbling over addresses that it was not supposed to write to. This of course is programmed by the OS device drivers.

The big I/O boards are also self-checking and contain a pair of everything. However, with the exception of the K600 they do not run lock-stepped to the twin FRU. For example on the K450/K460 boards, each of the SCSI host adapters is connected via the backplane into the same SCSI bus on the partner board, but each board’s controller occupies a different SCSI target ID. Only one controller is normally active, but when a failure occurs on the active board, all I/O is switched to the other controller. For the Ethernet ports on that board, they can be wired up to the same network or to different networks, and a software RNI (redundant network interface) layer provides transparent switching.

Other communications interfaces employ software-driven failover schemes.

All disks are mirrored. Early FTX 3.x releases used an in-house virtual disk layer (VDL) driver, but later releases switched to a modified version of the Veritas VxVM product. In HP-UX, HP’s own LVM (logical volume manager) is used. VOS, of course, has its own disk mirroring scheme.

The Continuum 400 series has the same CPU/memory architecture as the 600/1200, but the I/O bus is different. Instead of a Golf bus, it has an X bus that connects each CPU/memory module to a pair of PCI bridge boards. All I/O connectivity is via PCI cards. There are two PCI bays of 7 slots each, connected downstream from the PCI bridge boards. Each bay has a dual channel SCSI adapter on it as standard equipment. These are also cross-wired and dual-initiated much in the same way as the SCSI ports on the 600/1200 systems. The 400 is also typically shipped with a pair of Ethernet adapter cards. The PCI bridge boards also each contains a removable PCMCIA flash memory card. This is used as the boot device. FTX puts the bootloader as well as the UNIX kernel on there, whereas HP-UX only uses it for the bootloader.

The PCI bay doors control the power the the PCI slots. Once opened, all slots in that bay are powered off to facilitate removal and insertion of cards. The system continues to run on cards in the other bay. An interlock mechanism prevents both bay doors from being opened at the same time.

Again, all disks are mirrored as they are on the 600/1200 series, and communications interfaces use software-controlled failover mechanisms.

On the Continuum 400 the Console Controller is integrated into the CPU/memory FRUs. You can still reset the system via the software front panel on the console, but to power up/down you need to use the actual power switches on the machine (there are two, one for each power supply).

The Continuum 400 has two chassis versions, one is a short form-factor and AC powered only, and there is a tall CO (central office) version with a choice of AC or DC power. *(Thanks to Ti Kan for the input.)*

4.52.3 Operating systems

Operating system support was split between the Continuum 400 on the one hand and the Continuum 600 and 1200 on the other hand.

The Continuum 400 supported a Stratus-modified HP-UX Unix (11.00) and were marketed/offered with this system as main choice. The 400s also supported Stratus' own FTX Unix, which was only sold on an exceptional basis however. There also was a cancelled effort to port the Stratus VOS operating system to the 400s. Continuum 400 servers running the Stratus-modified HP-UX 11.00 were fully binary (ABI) compatible with stock HP HP-UX, that is, programs compiled for "normal" HP-UX ran without changes on Continuum 400s.

The Continuum 600 and 1200 in contrast were primarily being sold with Stratus' VOS operating system (non-Unix). VOS runs from release 13.0 until 14.7.2 on PA-RISC hardware.

"The original operating system developed for Stratus hardware was VOS. [...] VOS was designed from its inception as a high-security transaction- processing environment tailored to Fault-Tolerant hardware. It incorporates much of the design experience that came out of the famous MIT/Bell-Laboratories/General-Electric (later Honeywell) MULTICS project." *(See Note 7)*

Also offered on the 600s and 1200s—on an exceptional basis—was Stratus FTX, the System V Unix from Stratus. Hardware supports was however more limited than that of the "native" VOS on these systems.

4.52.4 System Table

Table 4.77: Stratus Continuum PA-RISC servers overview

Model	CPU	Logical/ Physical CPUs	Cache per CPU	RAM (max)	Expansion (max)	Storage (max)	I/O (max)	OS
419	PA-8500 360MHz	L1/P4	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
429	PA-8500 360MHz	L2/P8	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
439	PA-8600 480MHz	L1/P4	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
449	PA-8600 480MHz	L2/P8	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
610S	PA-7100 72MHz	L1/P4	512KB	128MB	6 slots			VOS, FTX
610	PA-7100 72MHz	L1/P4	512KB	512MB	6 slots			VOS, FTX
615S	PA-7100 96MHz	L1/P4	2MB	128MB	6 slots			VOS, FTX
615	PA-7100 96MHz	L1/P4	2MB	1GB	6 slots			VOS, FTX
616S	PA-8500 360MHz	L1/P4	1.5MB	0.5GB	6 slots			VOS, FTX

616	PA-8500 360MHz	L1/P4	1.5MB	2GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX
618	PA-8000 180MHz	L1/P4	2MB	3GB	6 slots			VOS, FTX
619	PA-8500 380MHz	L1/P4	1.5MB	4GB	6 slots			VOS, FTX
620	PA-7100 72MHz	L2/P8	512KB	512MB	6 slots			VOS, FTX
625	PA-7100 96MHz	L2/P8	2MB	2GB	6 slots			VOS, FTX
628	PA-8000 180MHz	L2/P8	2MB	3GB	6 slots			VOS, FTX
629	PA-8500 380MHz	L2/P8	1.5MB	4GB	6 slots			VOS, FTX
651-2	PA-8600 480MHz	L1/P4	1.5MB	4GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX
652-2	PA-8600 480MHz	L2/P8	1.5MB	4GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX
1210	PA-7100 72MHz	L1/P4	512KB	?	12 slots			VOS, FTX
1215	PA-7100 96MHz	L1/P4	2MB	?	12 slots			VOS, FTX
1218	PA-8000 180MHz	L1/P4	2MB	3GB	12 slots			VOS, FTX

1219	PA-8500 380MHz	L1/P4	1.5MB	4GB	12 slots			VOS, FTX
1220	PA-7100 72MHz	L2/P8	512KB	512MB	12 slots			VOS, FTX
1225	PA-7100 96MHz	L2/P8	2MB	2GB	12 slots			VOS, FTX
1228	PA-8000 180MHz	L2/P8	2MB	3GB	12 slots			VOS, FTX
1229	PA-8500 380MHz	L2/P8	1.5MB	4GB	12 slots			VOS, FTX
1245	PA-7100 96MHz	L4/P16	2MB	2GB	12 slots			VOS, FTX
1251-2	PA-8600 480MHz	L1/P4	1.5MB	4GB	18 PCI, 6 Stratus I/O, 84 I/O	L95/P190 disks, 4 tape drives	18 10/100Mbit, 8 T1/E1, 24 TR, 8 FDDI, 448 Async, 112 RS232, 84 X.21, 168 V.35	VOS, FTX
1252-2	PA-8600 480MHz	L2/P8	1.5MB	4GB	18 PCI, 6 Stratus I/O, 84 I/O	L95/P190 disks, 4 tape drives	18 10/100Mbit, 8 T1/E1, 24 TR, 8 FDDI, 448 Async, 112 RS232, 84 X.21, 168 V.35	VOS, FTX

Table Notes

- ◆ Logical/Physical CPUs: “L” and “P” denote *Logical* and *Physical* devices — logical CPUs are made up of two pairs of CPUs each (*i.e.*, 2×2)
- ◆ Storage: “L” and “P” denote *Logical* and *Physical* devices — logical disk drives are formed from physical devices via RAID sets
- ◆ I/O: Maximum number of I/O devices supported (not necessarily always configured with this number); notably the devices are also redundant

4.52.5 References

1. **The Stratus Continuum Family**²⁵⁴ (n.d.: Stratus Technologies Bermuda Ltd. Accessed 22 December 2007)
2. **The Stratus Continuum 400 Series**²⁵⁵ (n.d.: Stratus Technologies Bermuda Ltd. Accessed 22 December 2007)
3. **The Stratus Continuum 600 and 1200 Series**²⁵⁶, (n.d.: Stratus Technologies Bermuda Ltd. Accessed 22 December 2007)
4. **Stratus Machine History**²⁵⁷ (April 2007: Paul Green. Accessed 21 December 2007)
5. **Stratus Continuum Series - VOS, Stratus Virtual Operating system**²⁵⁸ (PDF, 49KB) (2003: Stratus Technologies Bermuda Ltd. Accessed 20 December 2007)
6. **Continuum 600/1200 Series (PA-7100) Service Announcement**²⁵⁹ (PDF, 288KB) (August 1998: Stratus Computer, Incorporated. Accessed 25 December 2007)
7. **Info-Stratus List Frequently Asked Questions periodical**²⁶⁰ (1998: Richard S. Shuford. Accessed 24 December 2007)

²⁵⁴<http://www.stratus.com/products/continuum>

²⁵⁵<http://www.stratus.com/products/continuum/s400>

²⁵⁶<http://www.stratus.com/products/continuum/s600>

²⁵⁷ftp://ftp.stratus.com/pub/vos/doc/reference/machine_history.txt

²⁵⁸<http://www.stratus.com/download/?file=/pdf/continuum/vosds.pdf>

²⁵⁹<http://www.stratus.ecacsupport.com/servicedocinternal/pdf/jettasa.pdf>

²⁶⁰<http://www.cs.utk.edu/~shuford/terminal/i-s.faq.periodic>

4.53 Hitachi PA-RISC systems

Hitachi²⁶¹ sold various PA-RISC computers in the 1990s, almost exclusively in Japan.

The Hitachi 3050RX workstations and 3500 servers are computers built around Hitachi (early systems) and HP PA-RISC processors, based on Hitachi system designs. These systems run Hitachi's HI-UX/WE2 operating system, an Unix version apparently compatible to standard HP-UX.

Later on Hitachi sold the 9000V OEM systems, rebranded HP 9000 workstations and servers, in Japan. This was part of Hitachi's membership in the Precision RISC organisation (PRO), combining several third-party vendors under the PA-RISC umbrella.

4.53.1 3050RX workstations

Comparable to HP's own 9000/700 series featuring small to medium sized workstations.

Model	Case	CPU	Cache (I/D)	RAM (max.)	Expansion
3050RX/100C	Laptop	Hitachi PA/50L	8/4KB	80MB	?
3050RX/200	Pizzabox	Hitachi PA/50M 33MHz	8/4KB	144MB	?
3050RX/220	Pizzabox	PA-7100 50MHz	64/64KB	192MB	None (Communication)
3050RX/225	?	PA-7100LC 60MHz	256KB	?	?
3050RX/230	Pizzabox	PA-7100 80MHz	256/256KB	192MB	None (Communication)
3050RX/235	?	PA-7100LC 80MHz	512KB	?	?
3050RX/255	Small	PA-7300LC 132MHz	64/64KB L1 (1MB L2)	256MB	Two slots
3050RX/310S	Desktop	PA-7100 33/40MHz	64/64KB L1	272MB	One slot
3050RX/320	Desktop	PA-7100 50MHz	64/64KB L1	416MB	Three slots
3050RX/320G (See Note 1)	Desktop	PA-7100 50MHz	64/64KB L1	192MB	Three slots
3050RX/320S	Desktop	PA-7100 50MHz	64/64KB L1	272MB	One slot
3050RX/330	Desktop	PA-7100 80MHz	256/256KB	416MB	Three slots
3050RX/330G (See Note 1)	Desktop	PA-7100 80MHz	256/256KB	192MB	Three slots
3050RX/330T (See Note 1)	Desktop	PA-7100 80MHz	256/256KB	192MB	Three slots
3050RX/330	Desktop	PA-7100 100MHz	256/256KB L1	416MB	Three slots
3050RX/355E	?	PA-7300LC 132MHz	64/64KB L1 (1MB L2)	1.5GB	Two slots One audio
3050RX/365	?	PA-7300LC 160MHz	64/64KB L1 (1MB L2)	1.5GB	Two slots One audio
3050RX/430	Deskside	PA-7100 80MHz	256/256KB L1	768MB	Seven slots
3050RX/440	Deskside	PA-7100 100MHz	256/256KB L1	768MB	Seven slots

²⁶¹<http://www.hitachi.com>

3050RX/535	?	PA-7100LC 80MHz	512KB LI	?	?
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Notes

1. “G” and “T” models included 3D graphics accelerators/processors, “T” models additionally HDTV.

4.53.2 3500 servers

Model	Case	CPU	Cache (I/D)	RAM(max.)	Expansion
3500/310	Desktop	PA-7100 50MHz	64/64KB	416MB	?
3500/410	Desktop	PA-7100 50MHz	64/64KB	512MB	?
3500/510	Desktop	PA-7100 50MHz	64/64KB	512MB	?
3500/520	Desktop	PA-7100 50MHz	256/256KB	512MB	?
3500/530	Desktop	PA-7100 80MHz	256/256KB	512MB	?
3500/540	Desktop	PA-7100 100MHz	256/256KB	512MB	?
3500/630	Cabinet	PA-7100 80MHz	256/256KB	1024MB	?
3500/640	Cabinet	PA-7100 100MHz	256/256KB	1024MB	?

4.53.3 9000V OEM systems

Hitachi also sold a line of original HP systems as OEM (probably only in Japan) — rebranded as “Hitachi 9000V series” which included the following systems from 1995 onwards:

- ◇ VQ200: HP 9000/J200
- ◇ VQ210: HP 9000/J210
- ◇ V735/125: HP 9000 735/125
- ◇ V715/100XC, V715/100, V715/80, V715/64: HP 9000/715 (newer models)
- ◇ V715/100Tiny, V715/80Tiny: probably HP 9000/712 (but not clear)
- ◇ VT500: HP 9000/T500 (T-Class)
- ◇ VR400: HP 9000/K400
- ◇ VR200: HP 9000/K200
- ◇ VR100: HP 9000/K100
- ◇ VE55, VE45, VE35, VE25: HP 9000/E-Class

4.53.4 Single systems details

3050RX/100C

A color laptop workstation using a PA/50L processor from Hitachi. RAM ranges from 16MB to 80MB, it included a 500MB internal hard drive and a XGA (1024×768) TFT display.

3050RX/200

A thin pizzabox-style workstation using a PA/50 processor from Hitachi, probably in the *M* version running at 33MHz. RAM ranges from 16MB to 144MB.

3050RX/225

A system with a PA-7100LC processor at 60MHz with 128/128KB off-chip cache. Released in mid-1994, SPECint92 of 65.2.

3050RX/235

A system with a PA-7100LC processor at 80MHz with 256/256KB off-chip cache. Released in mid-1994, SPECint92 of 91.1.

3050RX/255

Also a smaller workstation, but using a HP PA-7300LC processor at 132MHz with 64/64KB on-chip cache. RAM ranges from 64MB to 256MB, the machine has internal and external SCSI-2, external parallel, RS-232C, AUI-Ethernet. Two expansion slots are available. The integrated video adapter supports a maximum resolution of 1280×1024 with 8-bit colors. SPEC95 int/fp: 5.94/6.23.

3050RX/355E

A bigger workstation, also using a HP PA-7300LC processor at 132MHz with 64/64KB on-chip and optional 1MB external cache. RAM ranges from 64MB to 1536MB, the machine has internal and external SCSI-2, external parallel, 2 RS-232C, AUI-Ethernet. Two expansion slots and one audio slot are available. The integrated video-adapter supports a maximum resolution of 1280×1024 with 8-bit deep colors. With an option 1600×1280 with 24-bit color is possible. SPEC95 int/fp: 5.94/6.23.

3050RX/365

A bigger workstation, using a HP PA-7300LC processor at 160MHz with 64/64KB on-chip and optional 1MB external cache. RAM ranges from 64MB to 1536MB, the machine has internal and external SCSI-2, external parallel, 2 RS-232C, AUI-Ethernet. Two expansion slots and one audio slot are available. The integrated video-adapter supports a maximum resolution of 1280×1024 with 8-bit deep colors. With an option 1600×1280 with 24-bit color is possible. SPEC95 int/fp: 7.14/7.03.

4.53.5 References

1. **IPJS Computer Museum: 3050RX Hitachi Group/3500 Series**²⁶² [Google translation into English] Information Processing Society of Japan (n.d. Accessed August 2008) and

²⁶²<http://translate.google.com/translate?hl=en&sl=ja&u=http://museum.ipsj.or.jp/computer/work/0024.html>

4.54 HP 9000/500 FOCUS

(With Frank McConnell; some parts taken with permission from him)

4.54.1 Overview

The HP 9000/500s computers were the early-1980s predecessors of the PA-RISC workstations and the first member of the HP 9000 series. Although already based on a HP 32-bit processor — the FOCUS — they did not have PA-RISC CPUs.

The HP 9000/520 (originally 9020, the first 500 series) was introduced in 1982 by HP and one year later described in the Hewlett Packard Journal as “[...] the new HP 9000 computer, a mainframe on the desktop [...]”. All 500s used the same processors, memory and I/O; differences were in expandability and built-in I/O.

The HP 9000/500 series was withdrawn after several years (production stopped in 1989), probably due to the complexity and cost of its architecture (the five years younger first PA-RISC NMOS implementation had one third the FETs of the FOCUS processor).

4.54.2 Processors

The basic architecture of the 500 series was based on the Hewlett-Packard FOCUS architecture, implemented in five NMOS-III VLSI ICs (fabbed in 1.5 micron): the CPU chip, I/O processor (IOP), memory controller, 128Kb RAM (16KB cache) and clock driver.

The CPU ran at 18MHz and had a “direct address range” of “500MB” (probably 29-bit direct addressing for 512MB). It was fabricated with 450,000 FETs (integrated with three Floating-Point chips onto one “finstrate” CPU board). The FOCUS CPU was microcoded (9,000 38-bit microcode control stores) and implemented the HP 3000 computers’ stack-based architecture in 32-bit. All internal data paths and registers are 32-bit wide. Due to heat dissipation difficulties the ICs were mounted on special printed-circuit boards called “finstrates” — the board has a 1mm copper sheet as core to which the IC substrate is epoxied directly.

The I/O Processor (IOP) executes all I/O instructions and handles the transactions from/to the eight attached HP CIO channels. It has an I/O bandwidth of 5.1MB/s (burst) and 973KB/s (multiplexed). The IOP was also a microprogrammed (4,608 32-bit microcode stores) NMOS-III VLSI chip.

At least one IOP to interface with the I/O buses was needed so up to six CPUs were supported in hardware (but only three in software). Up to two additional IOPs could be installed for more I/O options; each additional IOP needed an I/O expander which provided the I/O channels extension (CIO bus).

The three finstrates boards (CPU, IOP and 256KB RAM) were installed in a 12-slot (HP 9000/520) module. This allowed configurations of up to 10MB of RAM; memory cards could be substituted to construct multiprocessor systems. The CPU, IOP and memory controller communicated via the memory processor bus (MPB). The 44-line, 18MHz, 36MB/s MPB supports up to seven (other sources mention three/three) CPUs or IOPs and fifteen memory controllers.

4.54.3 Systems

Four distinct models were introduced between 1982 and 1984 (all based on the same architecture):

HP 9000/520 *Dawn* (also HP 9020):

- ◇ Original desktop version
- ◇ Introduced 1982 for \$30,000
- ◇ One CPU (up to three supported)
- ◇ 512KB RAM (10MB maximum)
- ◇ One IOP (up to three supported)
- ◇ 5.25" floppy
- ◇ Optional 10MB hard drive
- ◇ 9020A: 12" color monitor with 512×390 resolution
- ◇ 9020B: 12" monochrome (green) monitor with 560×455 resolution
- ◇ 9020B: 13" color monitor with 560×455 resolution
- ◇ 9020AS (bundled system): 9020A with 1MB RAM, the optional 10MB hard drive, thermal printer, HP BASIC operating system
- ◇ 9020AT (bundled system): 9020A with 1.5MB RAM, thermal printer, HP-UX operating system (single-user)

HP 9000/530 *Corona* (also HP 9030):

- ◇ 19" rack-mount version (432×584×222mm w/h/d)
- ◇ Introduced 1982 for \$23,105
- ◇ One CPU (up to three supported)
- ◇ 512KB RAM (10MB maximum)
- ◇ One IOP (up to three supported)
- ◇ 9030A: base system (probably equals 9030)

HP 9000/540 *Corona* (also HP 9040):

- ◇ Free-standing cabinet system (356×711×711mm w/h/d)
- ◇ Introduced 1982 for \$24,115
- ◇ One CPU (up to three supported)
- ◇ 512KB RAM (10MB maximum)
- ◇ One IOP (up to three supported)
- ◇ 9040A: base system (probably equals 9040)
- ◇ 9040AT (bundled system): 9040A with 1.5MB RAM, HP-UX operating system (single-user)
- ◇ 9040AM (bundled system): 9040A with 1.5MB RAM, HP-UX operating system (multi-user)

HP 9000/550 *Shuttle* (also HP 9050):

- ◇ Industrial system (325×530×234mm w/h/d), similar in shape to HP 9000/300s
- ◇ Replaced 530 and 540

- ◊ Introduced 1984
- ◊ One CPU (up to three supported)
- ◊ 512KB RAM (10MB maximum)
- ◊ Up to four Display Station Buffer Cards (DSBs) [graphics adapters]
- ◊ One IOP (up to two supported)
- ◊ HP-IB interface (“medium-speed”)
- ◊ 9050A: base system (probably equals 9050)
- ◊ 9050AT (bundled system): 9050A with 1.5MB RAM, HP-UX operating system (single-user)
- ◊ 9050AM (bundled system): 9050A with 1.5MB RAM, HP-UX operating system (multi-user)

HP 9000/500s in SMP configuration were confusingly also called *600 series* (some of the 1980s' 800s server systems were also called 600 series for a short time).

Possible I/O and expansion options (for all 500s):

- ◊ HP-IB card for external HP-IB (HP Instrumentation Bus) devices
- ◊ GP-IO card for GP-IO (General Purpose I/O) devices with 8-bit or 16-bit DMA
- ◊ Asynchronous Serial
- ◊ I/O Expander for eight I/O channels/slots (CIO) for additional IOPs
- ◊ LAN 9000, 10Mbit Ethernet (coax)

4.54.4 Architecture

The FOCUS is a stack architecture, with 230 instructions (both 32 bits and 16 bits wide), a segmented memory model, and no general purpose programmer-visible registers. There are thirty-nine 32-bit registers in the CPU hardware—thirty-one internal 32-bit general purpose registers, two 32-bit ALU registers, and others.

It has a flat address space but that is not really what most programs see: their access to memory is largely described by registers that contain the absolute memory addresses of segment boundaries. For example, instructions come from the current code segment, which is described by three registers: **P**, the program counter, which is a 32-bit register containing the absolute address of the instruction being executed; **PB**, the program base register, which is a 32-bit register containing the absolute address of the first word of the current code segment; and **PL**, the program limit register, which is a 32-bit register containing the absolute address of the last word of the current code segment.

The data segment also has base (**DB**) and limit (**DL**) registers, and so does the stack segment (**SB**, **SL**). The stack segment also has a stack pointer (**S**) and a stack marker pointer (**Q**) which points to the current procedure's activation record on the stack.

There is also an index register, a status register, a flags register (really a sort of debugging-state register), a message register (interrupting conditions) and message mask register (which enables/disables interrupts from the message register), a breakpoint register, and a couple of registers which are for the memory controllers to talk to the CPU.

The machine instruction set is oriented toward moving words between memory and the top of the stack, and operating on the words at the top of the stack. To take an addition of two numbers: load

one, load the other, execute an **ADD** instruction, and then a store instruction if the result should be kept somewhere in memory other than on the stack.

The stack is in memory, there are (probably) some numbers of “top of stack” registers inside the processor to keep things moving relatively quickly, but these registers are not otherwise visible to the programmer.

4.54.5 Software

A choice of operating systems was provided by HP for the 520: HP BASIC or HP-UX. All other 500s (530, 540 and 550) only supported HP-UX. The operating systems were built on top of a common kernel, called **SUNOS** (no relation to Sun Microsystems’ SunOS Unix) which provided basic operating primitives like memory, processor and I/O management. This was intended to be invisible to the user; the Unix operating system on top ran as a single process on it. SUNOS was not a single binary image, compile-time switches allowed for BASIC and HP-UX builds. HP-UX ran until version 5.3 on HP FOCUS hardware.

There were three revision of SUNOS:

SUN I OS:

- ✧ Kernel for BASIC language system on Dawn (the 9000/520)
- ✧ Single user
- ✧ No virtual memory
- ✧ Supports only HP “Focus” (*i.e.*, HP’s own) memory boards
- ✧ Only for HP 9000/520

SUN II OS:

- ✧ Supports both HP BASIC and HP-UX (at that time a port of System III Unix)
- ✧ Multiple users
- ✧ Virtual memory
- ✧ Supports only HP “Focus” (*i.e.*, HP’s own) memory boards
- ✧ For HP 9000/520, 530 and 540

SUN III OS:

- ✧ Updates for new hardware
- ✧ Multiple users
- ✧ Virtual memory
- ✧ Supports both HP “Focus” (*i.e.*, HP’s own) and commercial third-party memory boards
- ✧ For HP 9000/520, 530, 540 and 550

HP-UX for the 9000/500 was the first commercial UNIX supporting a multi-processor, multi-user system.

4.54.6 References

Manuals

- ◇ HP 9000 Series 500 Computers Models 520, 530, 540, 550 Hardware Technical Data²⁶³ (.pdf) Hewlett Packard (November 1984. Accessed 15 January 2008 at hpmuseum.net)
- ◇ 9050 CE Handbook for the HP 9000 Series 500²⁶⁴ (.pdf) Hewlett-Packard Company (1985. Accessed 15 January 2008 at hpmuseum.net)
- ◇ OVERVIEW SUN III O.S., Hewlett Packard (Version 1.0/September 1984: Hewlett Packard)

Articles

- ◇ An 18-MHz, 32-bit VLSI Microprocessor²⁶⁵ (.pdf, pp. 7-10) Kevin P. Burkhart (August 1983. Hewlett Packard Journal. Accessed 15 January 2008 at hpmuseum.net)

Other

- ◇ Hewlett-Packard 9000 Series 520²⁶⁶ Frank McConnell (1997. Accessed January 2008)
- ◇ HP Computer Museum - Technical Desktops - 9000/520²⁶⁷ Jon Johnston (n. d.: WordSong Communications P/L. Accessed 15 January 2008)
- ◇ Re: HP 9000/500 vs. Vectra with 386 CPU and 387 co-processor?²⁶⁸ Roger N. Clark (28 July 1988: USENET posting comp.sys.hp)

²⁶³<http://www.hpmuseum.net/document.php?catfile=32>

²⁶⁴<http://www.hpmuseum.net/document.php?catfile=154>

²⁶⁵<http://www.hpmuseum.net/document.php?catfile=82>

²⁶⁶<http://www.reanimators.org/vcf/hp9k520.html>

²⁶⁷http://www.hpmuseum.net/display_item.php?hw=367

²⁶⁸<http://groups.google.com/group/comp.sys.hp/msg/bde9of241aeff8c1?dmode=source>

Chapter 5

Appendix

5.1 Bibliography

Systems

- ◇ HP 9000 Model 712 Overview (<http://www.hpl.hp.com/hpjjournal/>" "95apr/apr95a1.pdf) (PDF, HP Journal 4/95)
- ◇ Product design of the Model 712 (<http://www.hpl.hp.com/hpjjournal/95apr/apr95a9.pdf>) (PDF, HP Journal 4/95)
- ◇ Model 712 Technical Reference (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37629/lpv37629.pdf>) (PDF, 3.7MB)
- ◇ Model 712 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37944/lpv37944.pdf>) (PDF, 4.4MB)
- ◇ Model 715 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37699/lpv37699.pdf>) (PDF, 5.1MB)
- ◇ Model 735 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38563/lpv38563.pdf>) (PDF, 7.6MB)
- ◇ Model 720/730 owner's guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37630/lpv37630.pdf>) (PDF, 1.8MB)
- ◇ 743 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/>" "SupportManual/lpv38556/lpv38556.pdf) (PDF, 1.8MB)
- ◇ 743, 744 and 748 Technical Reference Manual (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00265/lpv00265.pdf>) (PDF, 2.2MB)
- ◇ Installing the A4505A PCI Module Upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00284/lpv00284.pdf>) (PDF, 0.3MB)
- ◇ Installing the A4504A PMC Bridge Adapter and A4509A Expansion Adapter (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00276/lpv00276.pdf>) (PDF, 0.6MB)
- ◇ Installing Model 743 RAM Boards (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00298/lpv00298.pdf>) (PDF, 0.2MB)
- ◇ 744 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00271/lpv00271.pdf>) (PDF, 1.4MB)
- ◇ Installing Model 744 RAM Cards (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00274/lpv00274.pdf>) (PDF, 0.3MB)
- ◇ VME Services for HP-UX 10 and 11 (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00267/lpv00267.pdf>) (PDF, 1.3MB)
- ◇ 745i/747i Industrial Workstations Owner's Guide (http://www.hp.com/products1/vmesystems/support/doc_vme/A2628-90014.pdf) (PDF, 1.6MB)
- ◇ 742i Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00299/lpv00299.pdf>) (PDF, 1.5MB)
- ◇ A180 User's Manual (<http://docs.hp.com/hpux/pdf/Aclassdoc00.pdf>) (PDF, 0.9MB)
- ◇ B-Class Low-Cost Workstation description (<http://www.hpl.hp.com/hpjjournal/97jun/jun97a11.pdf>) (PDF, HP Journal 7/97)
- ◇ B-Class Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37741/lpv37741.pdf>) (PDF, 1.5MB)
- ◇ B-Class Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37927/lpv37927.pdf>) (PDF, 0.9MB)
- ◇ B1000/C3x00 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37930/lpv37930.pdf>) (PDF, 4.9MB)
- ◇ B1000/C3x00 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37739/lpv37739.pdf>) (PDF, 3.2MB)
- ◇ B2000 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37671/lpv37671.pdf>) (PDF, 8.8MB)
- ◇ B2000 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37670/lpv37670.pdf>) (PDF, 2.6MB)
- ◇ B2600 Technical Reference Manual (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38239/lpv38239.pdf>) (PDF, 33.0MB)
- ◇ C100/110 Owners Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37672/lpv37672.pdf>) (PDF, 1.6MB)
- ◇ C100/110 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37947/lpv37947.pdf>) (PDF, 1.5MB)
- ◇ C160L Owners Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37959/lpv37959.pdf>) (PDF, 1.6MB)
- ◇ C-Class Service handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37954/lpv37954.pdf>) (PDF, 1.6MB)
- ◇ C100 to C110 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37945/lpv37945.pdf>) (PDF, 0.2MB)
- ◇ C100, C110 to C160L CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37952/lpv37952.pdf>) (PDF, 0.5MB)
- ◇ C100, C110 to C160, C180 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37949/lpv37949.pdf>) (PDF, 0.5MB)
- ◇ C160 to C180 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37957/lpv37957.pdf>) (PDF, 0.2MB)

- ◇ C100, C110, C160, C180 to C200 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf>) (PDF, 0.5MB)
- ◇ C200 to C240 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37960/lpv37960.pdf>) (PDF, 0.2MB)
- ◇ C200, C240 to C360 CPU upgrade (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37961/lpv37961.pdf>) (PDF, 0.2MB)
- ◇ Development of a Low-Cost, High-Performance, Multiuser Business Server System (<http://www.hpl.hp.com/hpjournal/95apr/apr95a9.pdf>) (PDF, HP Journal 4/95)
- ◇ HP Workstation c8000 Technical Reference Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00093136/c00093136.pdf>) (PDF, 2.7MB)
- ◇ HP c8000 data sheet (<http://www.hp.com/workstations/risc/c8000/c8000.pdf>) (PDF, 400KB)
- ◇ D-Class Entry Server description (<http://www.hpl.hp.com/hpjournal/97jun/jun97a10.pdf>) (PDF, HP Journal 7/97)
- ◇ D-Class and R-Class Installation Guide (<http://docs.hp.com/hpux/pdf/A3262-90057.pdf>) (PDF, 0.4MB)
- ◇ D-Class and R-Class Operator's Guide (<http://docs.hp.com/hpux/pdf/A3262-90013.pdf>) (PDF, 1.1MB)
- ◇ D-Class and R-Class System Upgrade Guide (<http://docs.hp.com/hpux/pdf/A3262-90010.pdf>) (PDF, 0.9MB)
- ◇ J200, J210 technical reference manual (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37962/lpv37962.pdf>) (PDF, 2.6MB)
- ◇ J280 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37675/lpv37675.pdf>) (PDF, 6.3MB)
- ◇ J280 workstation upgrade instructions (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38001/lpv38001.pdf>) (PDF, 1.9MB)
- ◇ J280, J282, J2240 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37964/lpv37964.pdf>) (PDF, 6.8MB)
- ◇ J282, J2240 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37966/lpv37966.pdf>) (PDF, 3.1MB)
- ◇ J282 workstation upgrade instructions (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37965/lpv37965.pdf>) (PDF, 2.3MB)
- ◇ J2240 workstation upgrade instructions (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37963/lpv37963.pdf>) (PDF, 1MB)
- ◇ J5x00/J7x00 Owner's Guide (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37967/lpv37967.pdf>) (PDF, 4.5MB)
- ◇ J5x00/J7x00 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37674/lpv37674.pdf>) (PDF, 4.4MB)
- ◇ J6000 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37677/lpv37677.pdf>) (PDF, 4.5MB)
- ◇ J6000 Technical Reference (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37634/lpv37634.pdf>) (PDF, 3.3MB)
- ◇ J6700 Service Handbook (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37640/lpv37640.pdf>) (PDF, 9.8MB)
- ◇ J6700 Technical Reference (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37641/lpv37641.pdf>) (PDF, 5.6MB)
- ◇ K-Class Installation Guide (HP 9000/Kxx0) (<http://docs.hp.com/hpux/pdf/A2375-90006.pdf>) (PDF)
- ◇ K-Class Installation Guide (HP 3000/9x9KS) (<http://docs.hp.com/hpux/pdf/A2375-90005.pdf>) (PDF)
- ◇ K-Class Owner's Guide (<http://docs.hp.com/hpux/pdf/A2375-90003.pdf>) (PDF)
- ◇ K-Class System Upgrade Manual (<http://docs.hp.com/hpux/pdf/A2375-90011.pdf>) (PDF)
- ◇ (L1000/L2000) rp5400 User Guide (<http://www.docs.hp.com/hpux/pdf/A5191-96018.pdf>) (PDF)
- ◇ (L1500/L3000) User Guide rp5400 Family of Servers (<http://docs.hp.com/en/A5191-96018/A5191-96018.pdf>) (PDF) Hewlett-Packard Company (November 2002, first edition)
- ◇ (L1500/L3000) *hp server rp5400 series entry-level UNIX servers technical whitepaper*, Hewlett-Packard Company (August 2002) [did not find an appropriate URL for this PDF document — Ed.]
- ◇ HP Workstation i2000 Owner's Guide (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpv37642/lpv37642.pdf>) (PDF) Hewlett-Packard Company (May 2001, first edition)
- ◇ (N4000) *hp server rp7410 whitepaper*, Hewlett-Packard Company (March 2002, product number 5980-9997EN) [did not find an appropriate URL for this PDF document — Ed.]
- ◇ (N4000) User Guide hp rp7405/7410 Servers <http://docs.hp.com/en/A6752-96008/A6752-96008.pdf> (PDF) Hewlett-Packard Company (2002, third edition)
- ◇ User Service Guide HP 9000 rp3410 and HP 9000 rp3440 <http://docs.hp.com/en/A7137-96008/A7137-96008.pdf> (PDF) Hewlett-Packard Development Company (April 2007, fourth edition)
- ◇ Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers <http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf> (PDF, 700KB) Hewlett-Packard (2005)
- ◇ User Service Guide HP 9000 rp4410 and HP 9000 rp4440 <http://docs.hp.com/en/A9950-96011/A9950-96011.pdf> (PDF) Hewlett-Packard Development Company (April 2007, third edition)
- ◇ Overview of the HP Integrity rx1600, rx2600, rx4640, and rx5670 servers technical whitepaper (<http://www.nitrosystem.com>)

- com/pdf/rx_servers_wp_01-23-04.pdf) (PDF) Hewlett-Packard Development Company (January 2004, second edition, 5982-1595EN)
- ◆ **Overview of the HP Integrity rx1600-2, rx2600-2, and rx4640-8 servers technical whitepaper** (http://h71028.www7.hp.com/ERC/downloads/rx4640_2600_1600_wp_FINAL_4-14-04.pdf) (PDF) Hewlett-Packard Development Company (April 2004, 5982-5031EN)
- ◆ **Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers** (<http://h71028.www7.hp.com/ERC/downloads/5982-9835EN.pdf>) (PDF) Hewlett-Packard Development Company (December 2006, rev. 4, 5982-9835EN)
- ◆ **hp Integrity rx1600 Operation and Maintenance** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404636/co1404636.pdf>) (PDF) Hewlett-Packard Development Company (January 2004)
- ◆ **hp Integrity rx1620 Operations Guide** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404664/co1404664.pdf>) (PDF) Hewlett-Packard Development Company (February 2005, AB430-96005)
- ◆ **hp Integrity rx1620 Maintenance Guide** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404656/co1404656.pdf>) (PDF) Hewlett-Packard Development Company (February 2005, AB430-96006)
- ◆ **Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpno4096/lpno4096.pdf>) (PDF) Hewlett-Packard Development Company (September 2003, second edition)
- ◆ **User Service Guide HP Integrity rx2620 Server** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404139/co1404139.pdf>) (PDF) Hewlett-Packard Development Company (August 2006, first edition, AD117-9003A)
- ◆ **hp server rx4610 User Guide** (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/coo112381/coo112381.pdf>) (PDF) Hewlett-Packard Company (n. d., version 0501)
- ◆ *An overview of the Itanium-based hp rx4610 server whitepaper*, Hewlett-Packard Company (June 2001, product number 5980-6420EN) [did not find an appropriate URL for this PDF document — Ed.]
- ◆ **User Service Guide HP Integrity rx4640 Server** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/co1404141/co1404141.pdf>) (PDF) Hewlett-Packard Development Company (August 2006, first edition, A6961-96013)
- ◆ **PrecisionBook hardware reference guide** (<ftp://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-refguide.pdf>) (PDF, 2.0MB)
- ◆ **PrecisionBook user guide** (<ftp://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-userguide.pdf>) (PDF, 1.4MB)
- ◆ **RDI software for HP-UX 10.20 installation guide** (<ftp://ftp.tadpole.com/support/Precisionbook/Manuals/hpux-10-2-installation-guide.pdf>) (PDF, 0.8MB)
- ◆ **RDI software release notes** (<ftp://ftp.tadpole.com/support/Precisionbook/Manuals/rdi-software-release-notes.pdf>) (PDF, 0.1MB)
- ◆ **HP Workstation zx2000 - Technical Reference Guide** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpv00324/lpv00324.pdf>) (PDF) Hewlett-Packard Development Company (April 2003, first edition)
- ◆ **Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000** (<http://bizsupport.austin.hp.com/bc/docs/support/SupportManual/lpno4096/lpno4096.pdf>) (PDF) Hewlett-Packard Development Company (September 2003, second edition)

CPU's

- ◆ **PA7100LC ERS (External Reference Specification)** (http://ftp.parisc-linux.org/docs/chips/PCXL_ers.pdf) (PDF, 410KB) Detailed official description of the PA-7100LC processor and its microarchitecture. Hewlett-Packard Company, 1999.
- ◆ **Design of the HP PA 7200 CPU** (http://ftp.parisc-linux.org/docs/whitepapers/pa7200_design.pdf) (PDF, 170KB) Overview on the PA-7200 internals and memory/cache architecture. Kenneth K. Chan et al, February 1996, Hewlett-Packard Journal.
- ◆ **A Different Kind of RISC** (<http://www.byte.com/art/9408/sec11/art3.htm>) PA-7200 general overview. Dick Pountain, August 1994, BYTE Journal.
- ◆ **PA7300LC ERS (External Reference Specification)** (http://ftp.parisc-linux.org/docs/chips/pcxl2_ers.pdf) (PDF, 716KB) Detailed official description of the PA-7300LC processor and its microarchitecture. Hewlett-Packard Company, 1996.
- ◆ **The PA-7300LC: the first "System on a Chip"** (http://web.archive.org/web/20040214111649/http://www.cpus.hp.com/technical_references/101995wp.shtml) (archive.org mirror) Presentation prepared for Microprocessor Forum 1995 summarizing the PA-7300LC. Tom Meyer, 1996.
- ◆ **The PA 7300LC Microprocessor: A Highly Integrated System on a Chip** (http://ftp.parisc-linux.org/docs/whitepapers/pa7300lc_on_chip.pdf) (PDF, 50KB). Shorter summary of the PA-7300LC's design objectives and goals. Terry W. Blanchard and Paul G. Tobin, June 1997, Hewlett-Packard Journal.
- ◆ **Advanced Performance features of the 64-bit PA-8000** (http://web.archive.org/web/20040214092531/http://www.cpus.hp.com/technical_references/advperf.shtml) (archive.org mirror) Detailed description of the PA-8000 innards, presented at CompCon 95. Doug Hunt, 1995, IEEE CS Press. (Article reprint for vanished cpus.hp.com)
- ◆ **PA-8000 Combines Complexity and Speed** (http://web.archive.org/web/20040214122429/http://www.cpus.hp.com/technical_references/111994ar.shtml) (archive.org mirror) More general introduction to the PA-8000. Linley Gwennap, 1994, Microprocessor Report, Volume 8 Number 15. (Article reprint for vanished cpus.hp.com)

- ◇ **Four-Way Superscalar PA-RISC Processors** (http://ftp.parisc-linux.org/docs/whitepapers/four_way_superscalar.pdf) (PDF, 190KB) Overview on PA-8000 and its predecessor PA-8200 with an eye on their execution capabilities. Anne P. Scott et al, August 1997, Hewlett-Packard Journal.
- ◇ **HP Pumps Up PA-8x00 Family** (http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml) (archive.org mirror) Description and results of the improvements made in PA-8200 and PA-8500. Linley Gwennap, October 1994, Microprocessor Report, Volume 10 Number 14. (Article reprint for vanished cpu.hp.com)
- ◇ **A 500 MHz 1.5 MByte Cache with On-Chip CPU** (http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk.pdf) (PDF, 141KB) Slides of a presentation on the PA-8500 CPU. Jonathan Lachman and J. Michael Hill, 1997, ISSCC.
- ◇ **PA-8500: The Continuing Evolution of the PA-8000 Family** (http://web.archive.org/web/20040214131135/http://www.cpus.hp.com/technical_references/8500.shtml) (archive.org mirror) Description of PA-8500 development and technical details. Gregg Lesartre and Doug Hunt, 1997, Proceedings of CompCon, IEEE CS Press. (Article reprint for vanished cpu.hp.com)
- ◇ **A 900MHz 2.25MByte Cache with On Chip CPU** (http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk_2.pdf) (PDF, 119KB) Slides of a presentation on the PA-8700 CPU, centered on the CPUs cache subsystem. J. Michael Hill and Jonathan Lachman, 2000, ISSCC.
- ◇ **HP Assembler Reference Manual** (<http://docs.hp.com/hpux/onlinedocs/92432-90012/92432-90012.html>) (HTML)
- ◇ **HP Assembler Reference Manual** (<http://docs.hp.com/hpux/pdf/92432-90012.pdf>) (PDF, 309KB)
- ◇ **Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers** (<http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf>) (PDF, 700KB) Technical Whitepaper from HP on new servers and PA-8900 processor. Hewlett-Packard, 2005.
- ◇ Wayne E. Holt (ed.), *Beyond RISC! An Essential Guide to Hewlett-Packard Precision Architecture* (January 1988: Software Research Northwest Inc.)
- ◇ **Hardware Design of the First HP Precision Architecture Computers¹** (PDF) David A. Fotland et al (March 1987: Hewlett-Packard Journal)
- ◇ **HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook²** (PDF) Hewlett-Packard Company (October 1990. Accessed January 2008 at hpmuseum.net)
- ◇ **HP 9000 Series 800 Model 825S Hardware Technical Data³** (PDF) Hewlett-Packard Company (September 1988. Accessed January 2008 at hpmuseum.net)
- ◇ **HP 3000/925 and HP 9000/825/835 Computer Systems CE Handbook⁴** (PDF) Hewlett-Packard Company (May 1988. Accessed January 2008 at hpmuseum.net)
- ◇ **New midrange members of the Hewlett-Packard Precision Architecture Computer Family⁵** Thomas O. Meyer et al (June 1989: Hewlett Packard Journal. Accessed January 2008 at findarticles.com)
- ◇ **HP 9000 Series 800 Model 822S/832S Technical Data⁶** (PDF) Hewlett-Packard Company (1989. Accessed January 2008 at hpmuseum.net)

Chipsets

- ◇ **Hardball ERS** (http://ftp.parisc-linux.org/docs/chips/hardball_ers.pdf) (PDF)
- ◇ **LASI ERS** (http://ftp.parisc-linux.org/docs/chips/lasi_ers.pdf) (PDF)
- ◇ **Dino ERS** (http://ftp.parisc-linux.org/docs/chips/dino_ers.pdf) (PDF)
- ◇ **Astro ERS Overview** (http://ftp.parisc-linux.org/docs/chips/astro_intro.pdf) (PDF)
- ◇ **Astro ERS Error Handling** (http://ftp.parisc-linux.org/docs/chips/astro_errors.pdf) (PDF)
- ◇ **Astro ERS R2I Operations** (http://ftp.parisc-linux.org/docs/chips/astro_ioc.pdf) (PDF)
- ◇ **Astro ERS Register Map** (http://ftp.parisc-linux.org/docs/chips/astro_regmap.pdf) (PDF)
- ◇ **Astro Runway Interface** (http://ftp.parisc-linux.org/docs/chips/astro_runway.pdf) (PDF)
- ◇ **Astro Memory Map** (http://ftp.parisc-linux.org/docs/chips/astro_sysmap.pdf) (PDF)
- ◇ **Elroy ERS** (http://ftp.parisc-linux.org/docs/chips/elroy_ers.pdf) (PDF)
- ◇ **LSI 53C875E** (http://www.lsilogic.com/techlib/marketing_docs/storage_stand_prod/integrated_circuits/l53c875e_pb.pdf) (PDF, 0.3MB)
- ◇ **LSI 53C896** (http://www.lsilogic.com/techlib/marketing_docs/storage_stand_prod/integrated_circuits/l53c896_pb.pdf) (PDF, 0.2MB)
- ◇ **Design of the Model 712's I/O subsystem (LASI)** (<http://www.hpl.hp.com/hpjjournal/95apr/apr95a4.pdf>) (PDF, HP Journal 4/95)
- ◇ **Runway Bus introduction** (<http://www.hpl.hp.com/hpjjournal/96feb/feb96a2.pdf>) (PDF, HP Journal 2/96)

¹ <http://hpmuseum.net/document.php?catfile=372>

² <http://www.hpmuseum.net/document.php?hwfile=4049>

³ <http://www.hpmuseum.net/document.php?hwfile=3343>

⁴ <http://www.hpmuseum.net/document.php?hwfile=4048>

⁵ http://findarticles.com/p/articles/mi_moHPJ/is_n3_v40/ai_7397316

⁶ <http://www.hpmuseum.net/document.php?hwfile=2652>

- ◇ **J/K-Class Memory System description** (<http://www.hpl.hp.com/hpjournal/96feb/feb96a5.pdf>) (PDF, HP Journal 2/96)
- ◇ **VISUALIZE Workstation Memory Subsystem** (<http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf>) (PDF, 120KB)

Miscellaneous Hardware

- ◇ **ADTX IDE-SCSI adapters** (<http://mickey.lucifer.net/adtx/>), as used in the RDI PrecisionBook
- ◇ **NetBSD 712 serial console HOWTO** (<http://www.netbsd.org/Ports/hp700/serialconsole-712.html>), instructions to configure your 712 to use serial console
- ◇ **Replacing the EEPROM on an HP J282** (<http://www.lava.net/~kirill/j282/eeprom.html>) (HTML). In case your J-Class needs a new EEPROM chip.

5.2 Changes

Changes in Second Edition 2.2 since Second Edition 2.1:

- ✧ Removal of several outdated pages: PDC Boot-ROM (only relevant to older systems, incomplete), LED error codes (same), Expansion cards (outdated and incomplete, just a collection of HP part numbers) and Memory modules (same)
- ✧ Almost all other pages have been updated and/or rewritten, especially the hardware sections (processors, chipsets, buses)

Changes in Second Edition 2.1 (October 2008) since Second Edition 2.0 (22 pages added):

- ✧ Convex Exemplar SPP1000, SPP1200 and SPP1600 (XA and CD) mainframes added
- ✧ HP/Convex Exemplar SPP2000 (S-Class/X-Class) mainframes added
- ✧ 3rd party PA-RISC computers information added: more Hitachi (3050RX, 3500 and 9000V OEM) and Mitsubishi (MELCOM ME RISC) and Oki (OKITAC 9000) OEM systems (relabelled HP)
- ✧ HP 9000/V2200 and V2250 Exemplar mainframes added
- ✧ HP 9000/V2500 and V2600 Exemplar mainframes added
- ✧ Cover page and several post-release spelling corrections

Changes in Second Edition 2.0 (May/June 2008) since First Edition 1.2 (about 90 pages added and almost all other updated/modified):

- ✧ HP Itanium/IA64 servers added: rx1600/rx1620, rx2600/rx2620, rx4610, rx4640 and rx5670
- ✧ HP Itanium/IA64 workstations added: i2000, zx2000 and zx6000
- ✧ Much improved Other PA-RISC Operating Systems page (Mach 4/Lites, HPBSD, OSF/1, Mach 3, Chorus, and others)
- ✧ HP 9000 N4000 (rp7400) server section added
- ✧ Stretch and Cell-based (Superdome) chipset sections added
- ✧ HP 9000 N4000 (rp7405 and rp7410) server section added
- ✧ HP 9000 L1500 (rp5430) and L3000 (rp5470) server section added
- ✧ HP 9000 rp3410 and rp3440 (*rp3400 series*) server section added
- ✧ HP 9000 rp4410 and rp4440 (*rp4400 series*) server section added
- ✧ Reworked and more detailed HP 9000/500 FOCUS systems section
- ✧ Expanded and corrected early PA-RISC history/servers section
- ✧ Early PA-RISC 1.0 processors (TS-1, NS-1, NS-2, CMOS26B/PCX) section added
- ✧ Much improved and expanded Stratus Continuum servers section
- ✧ Winbond W89K and W90K embedded PA-RISC processors section added
- ✧ Synchronize with online OpenPA.net content

- ◊ Typographic polishing (T_EX and in the HTML sources)
- ◊ Improvements to and streamlining of the HTML-to-PDF conversion process
- ◊ Removal of (book-format) DIN A5 print format

Changes in Release 1.2 (December 2007) since First Edition 1.1:

- ◊ Typographic modifications for limited print edition

Changes in Release 1.1 (November 2007) since First (Prerelease) Edition 1.0:

- ◊ Text formatting and positioning
- ◊ Typographic improvements
- ◊ Addition of a (book-format) DIN A5 print format
- ◊ PA-RISC History page added, covering the early PA-RISC days
- ◊ Catch-up with all changes/updates from the OpenPA online edition (about one year worth of updates)

First (Prerelease) Edition 1.0 was published in July 2006.

5.3 PA-RISC Benchmarks

Assorted benchmark results, compiled with available **SPEC benchmark**⁷ results for PA-RISC and Itanium systems. Multi-processor configurations are noted (2P, 4P etc.), otherwise the results are from single-processor systems.

Results from three different benchmark sets: **SPEC92**⁸, **SPEC95**⁹ and **SPEC2000**¹⁰.

Table 5.1: PA-RISC computers assorted SPEC benchmarks results

Model	SPEC92 int/fp	SPEC95 int/fp	SPEC95 rate int/fp	SPEC2000 int/fp	SPEC2000 rate int/fp
705	21.9/33.0				
710	31.6/47.6	1.0/1.4			
712/60	67.0/85.3	2.1/2.7	18.7/23.9		
712/80	97.1/123.3	3.1/3.5	28.1/32.0		
712/100	117.2/144.2	3.8/4.1	33.8/36.3		
715/33	32.5/52.4	1.0/1.6			
715/50	49.2/78.8	1.5/2.5			
715/64	80.6/109.4	2.5/3.3			
715/75	82.6/127.2	2.5/3.8			
715/80	96.3/123.2	3.0/3.5			
715/100	115.1/138.7	3.8/4.0	30.0/38.3		
715/100XC	132.2/184.6	4.5/4.7	40.9/42.3		
720	36.4/58.2	1.2/2.0	14.1/18.2		
725/50		1.5/2.5			
725/75		2.5/3.8			
725/100		3.8/4.0			
730	47.8/75.4	1.5/2.3			
735/99		3.2/4.1	29.4/35.8		
735/125		4.0/4.6	36.3/40.9		
742i/50		1.5/2.5			
743i/64		2.5/3.3			
743i/100		3.8/4.0			
744/132L		6.4/6.7			
744/165L		7.9/7.6			
745i/50		1.5/2.5			
745i/100		3.2/4.1			
745/132L		6.4/6.7			
745/165L		7.9/7.6			
747i/50		1.5/2.5			
747i/100		3.2/4.1			
748i/64		2.5/3.3			
748i/100		3.8/4.0			
748/132L		6.4/6.7			
748/165L		7.9/7.6			
750	48.1/75.0	1.5/2.3			
755/99		3.2/4.0	29.4/35.8		
755/125		4.0/4.6	36.3/40.9		
A180					
A180C		9.2/8.6			
A500-5X (rp2450)				422/414	2P: 9.3/7.6
A500-7X (rp2470)				581/	6.74/ 2P: 12.9/

⁷ <http://www.spec.org>

⁸ <http://www.spec.org/cpu92/>

⁹ <http://www.spec.org/cpu95/>

¹⁰ <http://www.spec.org/cpu2000>

B132L		6.4/6.7	58.1/60.3		
B132L+		6.8/7.2	61.5/64.6		
B160L		7.7/7.6	69.7/68.1		
B180L+		9.2/9.4	83.0/84.8		
B1000		23.9/39.3	217/378		
B2000		31.8/52.4	286/472	332/357	3.8/4.1
B2600				403/440	4.7/5.1
C100		5.0/6.6	44.8/59.4		
C110		6.0/8.1	54.0/73.3		
C132L		6.4/6.7	58.1/60.3		
C160L		7.7/7.6	69.7/68.1		
C160		10.4/16.3	93.6/147		
C180		11.8/18.7	107/169		
C200		14.2/21.4	129/193		
C240		17.1/25.4	156/229		
C360		26.0/28.1	234/252		
C3000		31.8/52.4	287/471	313/321	
C3600		42.0/64.0	379/576	432/433	5.0/5.0
C3650				508/542	5.9/6.3
C3700				604/576	7.0/6.7
C3750				678/674	
C8000				1001?/	
D200	115/146	2.2/2.9	19.2/25.8		
D210	152/194	3.7/4.1	33.6/36.7		
D220		6.6/6.7	59.2/60.5		
D230		7.9/7.6	70.8/68.3		
D250	144/218	5.0/6.8	45.1/61.0 2P: 89.0/106		
D260			2P: 114/143		
D270		10.4/15.0	93.9/135 2P: 184/190		
D280		12.3/17.4	111/157 2P: 219/221		
D300	115/146	2.2/2.9	19.2/25.8		
D310	152/194	3.7/4.1	33.6/36.7		
D320		6.6/6.7	59.2/60.5		
D330		7.9/7.6	70.8/68.3		
D350	144/218	5.0/6.8	45.1/61.0 2P: 89.0/106		
D360			2P: 114/143		
D370		10.4/15.0	93.9/135 2P: 184/190		
D380		12.3/17.4	111/157 2P: 219/221		
D390		15.5/25.5			
E25	45.0/66.7				
E35	65.6/98.5				
E45	82.1/122.9				
E55	108.0/163.4				
F10	22.0/36.6				
F20	33.6/56.1				
F30	37.8/62.4				
G30					
H30					
I30					
G40	65.2/91.3				
H40					
I40					

G50 H50 I50	100.0/158.5				
G60 H60 I60	108.8/195.3				
G70 H70 I70	108.8/195.3				
Galaxy 1100 80MHz (SAIC)		3.1/3.5			
i2000 733MHz 2MB				/623	/7.2
i2000 733MHz 4MB					/577
i2000 800MHz 2MB				/655 2P: /658	/7.6 2P: /13.2
i2000 800MHz 4MB				365/610	
J200		5.0/4.5	44.8/61.3 2P: 64.5/105		
J210		6.0/5.4	54.0/73.4 2P: 77.5/126		
J210XC		6.4/5.7	57.6/81.5 2P: 82.8/142		
J280		11.8/19.3	107/174		
J282					
J2240		17.4/26.3	157/237 2P: 307/349		
J5000		32.5/54.0	302/486 2P: 579/744		
J5600		42.6/62.7	384/564 2P: 758/847		
J6000		42.6/62.7	384/564 2P: 758/847	441/433	2P: 9.7/8.0
J6700		57.6/85.9		603/581	2P: 13.4/10.5
J6750				676/651	2P: 14.9/11.5
J7000		32.5/54.0	302/486 2P: 579/744		
K100		4.9/6.8			
K200		4.9/6.8	44.3/61.2 2P: 87.9/117 4P: 174/198		
K210		5.9/8.1	53.3/73.4 2P: 106/140 4P: 210/238		
K220		6.4/9.1	57.7/82.0 2P: 114/157 4P: 228/275		
K250		10.7/18.8	96.0/169 2P: 189/279 4P: 375/383		
K260		11.8/20.2	107/182 2P: 212/297 4P: 418/398		
K370		14.6/23.0	132/207 2P: 261/322 4P: 519/434 6P: 767/489		

K380		17.4/28.5	157/257 2P: 312/398 4P: 610/532 6P: 902/604		
K400		4.9/6.8	44.3/61.2 2P: 87.9/117 4P: 174/198		
K410		5.9/8.1	53.3/73.4 2P: 106/140 4P: 210/238		
K420		6.4/9.1	57.7/82.0 2P: 114/157 4P: 228/275		
K450		10.7/18.8	96.0/169 2P: 189/279 4P: 375/383		
K460		11.8/20.2	107/182 2P: 212/297 4P: 418/398		
K570		14.6/23.0	132/207 2P: 261/322 4P: 519/434 6P: 767/489		
K580		17.4/28.5	157/257 2P: 321/398 4P: 610/532 6P: 902/604		
L2000-44 (rp5450)		33.7/72.3			
L3000-5X rp2470				388/376	4.5/4.4 2P: 8.9/8.3 4P: 17.4/14.5
L3000-7X rp2470				581/	6.7/ 2P: 12.9/
N4000-6X rp7400				493/489	5.7/5.7 2P: 11.3/10.4 4P: 22.1/19.3 8P: 42.6/30.5
N4000-7X rp7400				551/524	6.4/6.1 2P: 12.5/11.0 4P: 24.6/20.5 8P: 46.7/32.1
PrecisionBook 132 (RDI)		6.5/6.5			
PrecisionBook 160 (RDI)		7.8/7.4			
PrecisionBook 180 (RDI)		9.2/9.4			
R380		12.3/17.4			
R390		15.5/25.5			
rp3440 1GHz dualcore					1P/2C: 18.7/19.2 2P/4C: 37.1/32.6
rp4440 1GHz dualcore					1P/2C: 18.6/19.3 2P/4C: 37.0/34.7 4P/8C: 73.2/55.4
rx1600 1.0GHz 1.5MB				837/1382	9.71/16.0 2P: 19.1/27.6
rx1620-2 1.3GHz 3.0MB				1178/2214	13.7/25.7 2P: 27.0/42.7

rx1620-2 1.6GHz 3.0MB				1452/2692	16.8/31.2 2P: 33.2/50.4
rx2600 900MHz 1.5MB				674/1151	7.8/ 2P: 15.5/
rx2600 1.0GHz 3.0MB				810/1427	9.4/ 2P: 18.7/
rx2600 1.3GHz 3.0MB				1073/1808	12.4/ 2P: 24.8/
rx2600 1.5GHz 6.0MB				1408/2119	15.3/ 2P: 30.5/
rx2620-2 1.3Hz 3.0MB				1170/2229	13.6/15.9 2P: 26.9/27.7
rx2620-2 1.6Hz 3.0MB				1408/2553	16.3/29.6 2P: 32.3/48.5
rx2620-2 1.6Hz 6.0MB				1535/2675	17.8/31.0 2P: 35.5/51.5
rx4610 800MHz 4MB				379/701	4.4/8.1 2P: /14.2 4P: /22.4
rx4640 1.3GHz 3.0MB				1132/1891	13.1/21.9 2P: 25.8/37.9 4P: 51.4/57.4
rx4640 1.5GHz 6.0MB				1404/2161	16.3/25.1 2P: 32.5/43.2 4P: 64.2/65.6
rx4640-8 1.5GHz 4.0?MB				1372/2502	15.9/29 2P: 31.7/48.3 4P: 62.2/70.5
rx4640-8 1.6GHz 9MB				1590/2712	4P: 72.5/77.9
rx5670 900MHz 1.5MB				673/1151	7.81/13.3 2P: 15.5/24.5 4P: 30.4/38.7
rx5670 1.0GHz 3.0MB				807/1431	9.36/16.6 2P: 18.6/30.7 4P: 36.8/49.3
rx5670 1.3GHz 3.0MB				1066/1814	12.4/21.0 2P: 24.5/37.3 4P: 48.6/57.2
rx5670 1.5GHz 6.0MB				1312/2108	1P: 15.2/24.5 2P: 30.3/42.6 4P: 60.0/66.4
T520		5.2/	1P: 47.2/ 2P: 93.8/ 4P: 186/ 8P: 363 12P: 531		
T600		11.8/14.9	1P: 106/134 2P: 211/263 4P: 418/510 6P: 617/735 8P: 814/915 10P: 1003/1043 12P: 1192/1151		
V2200		13.8/22.1	1P: 125/ 4P: 484/755 8P: 964/1380 12P: 1442/1909 16P: 1865/2312		
V2250		16.4/24.8	16P: 2209/2471		

V2500			16P: 4002 32P: 7481		
V2600			16P: 5164 32P: 9315		
SPP1000/XA (Convex)		3.3/4.0			
SPP1200/XA (Convex)	/185				
SPP1600/CD (Convex)			8P: 290/383 16P: 541/744 32P: 996/1444		
SPP2000 (Convex) S-Class X-Class		11.8/18.7	92.5/141 2P: 183/276 4P: 363/524 6P: 539/739 8P: 713/935 10P: 867/1085 12P: 1012/1220 16P: 1307/1413		
zx2000 900MHz				668/1086	/12.6
zx6000 900MHz				669/1139	7.8/13.2 2P: 15.4/23.9
zx6000 1.0GHz				807/1422	/16.5 2P: /30
zx6000 1.5GHz				1315/2106	15.2/24.4 2P: 30.4/42.4